Numerical and Symbolic Computational Approach to Design of LSI Circuits

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Graduate School of Humanities and Sciences,
Nara Women's University

Tamiyo NAKABAYASHI

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Abstract

In this thesis, we describe symbolic and numerical computational approach to design of LSI circuits as their industrial application. The objective of our research is to improve the efficiency and the accuracy of design by modeling the circuit behavior and characteristics based on equations and solving with symbolic or numerical computation in the early stages of LSI design.

In general, the designers describe the circuit structure based on constraints and specifications at first. Here, the circuit structure is the schematic or connection information of the circuit elements. Next, they give appropriate initial value for the parameters of the circuit elements and verify and analyze by simulation. They repeat the verification and analysis by simulation and adjust the parameters until they find the optimal design value. In order to improve the efficiency of the design, it is very important to know how each parameter impacts on their circuits properties. On the other hand, in order to converge the simulation, it is necessary to provide appropriate initial values, because the device model analysis formula implemented in the simulator is complicated and has strong nonlinearity.

In contrast, our proposed design approach is an equation-based method such that the circuit behavior and characteristics are represented as mathematical equations. By equation-based analysis of the circuit behavior and characteristics, it is possible to understand the effect of parameters on the properties quantitatively. Our proposed method is to model circuit behavior and characteristics by equations and solve them with constraints and specifications using generic symbolic computational system. The generic symbolic computational system has both symbolic and numerical calculation functions. Therefore we research the case of both symbolic and numerical calculation to obtain the solutions of the equations.

At first, we focus on importance of signal delay in digital design, and we apply the symbolic computation to estimate the signal delay. We model delay characteristic by a polynomial and design 1-bit full adder circuit by using proposed method. In addition, we expand to the analysis of the signal delay in consideration of the temperature rise due to Joule heating in interconnects. As a result, we confirm the effectiveness of our proposed method for the transient analysis that is the basis of the digital circuits design.

Next, we present two applications to frequency analysis that is very important in analog circuits design. The first application is to optimize the parameters of the power loop circuit that is a core of power supply system. We derive the transfer function of the power supply loop circuit and determine the most suitable circuit parameters to satisfy design target. To obtain these parameters, we try to solve a system of nonlinear equations by using symbolic and numerical computation. As a result, we obtain valid solutions with symbolic computation. The second application is to obtain design parameters of the DC/DC converter which is a representative power supply circuit. We derive the transfer function representing the behavior of whole system. In particular, we focus on that capacitance of the output capacitor and parasitic resistance among the design parameters have effects on the frequency characteristics and circuit stabilization of the DC/DC converter, so we apply our equation-based design and optimize design parameters with numerical computation. Our experimental results demonstrate that our technique makes possible to solve the case which cannot be solved by conventional power electronics circuit simulator. Also, calculation speed by our proposed method is 80 times faster than the conventional method, so our proposed method demonstrates the utility and efficiency.

Furthermore, we suggest a modeling of an equation-based electro-thermal coupling of power MOSFETs for predicting reliability by using numerical calculation. In view of this experimental result, we present that our proposed method is applicable to not only digital circuits transient analysis or analog circuits frequency analysis, but also power MOSFETS reliability evaluation.

Finally, we propose a technique for large scale power grid analysis with a parallel computing method in computer algebra system. We model a power grid as a system of ordinary differential

equations, and apply the parallel computing method to obtain the solution efficiently. We explain the technique using a linear RC elements network model as the power grid. Our experimental results demonstrate that the technique is capable of the time domain analysis just the same as SPICE, a general-purpose circuit simulator, and is applicable to power grid design of LSI chips. We also reveal the superiority of our technique for the power grids of very large scale, and also indicate the effectiveness of the parallel computing method in the power grid optimization design.

With our method, we achieve to improve the efficiency and the accuracy of design by modeling the circuit behavior and characteristics in the early stages of LSI design. In other words, we contribute to improve the efficiency and the accuracy in the semiconductor and LSI design field. Our proposed design method has generality and hence is applicable to any device, circuit, and system in semiconductor and LSI field. In addition, our method will lead to sharing and accumulation and acquisition of design knowledge between each designer.

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Chapter 1
Introduction

Computer algebra systems have significantly influenced scientific research in many fields, in particular mathematics, computer science, physics, chemistry, and engineering. They have supplemented the well-established numerical packages by new tools aimed at problems that require exact answers, or closed-form analysis of the dependence of a problem class on certain parameters. They offer a convenient environment for high-level programming of specialized algorithms involving complicated data-types. For example there is such as Maple [7] and Mathematica [8] as commercial tools, and Octave [12] and Scilab [15] as open source tools.

In the area of electronic/electrical circuits design, Mathematica is applied to the symbolic circuit analysis for analog circuits [1], [2], [5], [6]. The target of these researches is small signal analysis and transfer function modeling (frequency domain) for linear analog circuits, the circuits of which are composed of a number of resistors, capacitors, inductors, macro cells of operational amplifiers, and so on. Furthermore, in the Wolfram Demonstrations Project, some examples of equation-based modeling for very simple electronic circuits are exhibited [3].

In this thesis, we describe symbolic and numerical computational approach to the design of LSI circuits as their industrial application. The objective of our research is to improve the efficiency and the accuracy of design by modeling the circuit behavior and characteristics based on equations and solving with symbolic or numerical computation in the early stages of LSI design.

In general, the designers describe the circuit structure based on constraints and specifications at first. Here, the circuit structure is the schematic or connection information of the circuit elements. Next, they give appropriate initial value for the parameters of the circuit elements and verify and analyze by simulation. They repeat the verification and analysis by simulation and adjust the parameters until they find the optimal design value. In order to improve the efficiency of the design, it is very important to know how each parameter impacts on their circuits properties. On the other hand, in order to converge the simulation, it is necessary to provide appropriate initial values, because the device model analysis formula implemented in the simulator is complicated and has strong nonlinearity.

In contrast, our proposed design approach is an equation-based method such that the circuit behavior and characteristics are represented as mathematical equations. By equation-based analysis of the circuit behavior and characteristics, it is possible to understand the effect of parameters on the properties quantitatively. Our proposed method is to model circuit behavior and characteristics by equations and solve them with constraints and specifications using generic symbolic computational system. The generic symbolic computational system has both symbolic and numerical calculation functions. Therefore we research the case of both symbolic and numerical calculation to obtain the solutions of the equations.

With our method, we achieve to improve the efficiency and the accuracy of design by modeling the circuit behavior and characteristics in the early stages of LSI design. In other words, we contribute to improve the efficiency and the accuracy in the semiconductor and LSI design field. Our proposed design method has generality and hence is applicable to any device, circuit, and system in semiconductor and LSI field. In addition, our method will lead to sharing and accumulation and acquisition of design knowledge between each designer.

1.1 Digital circuits Design and Analysis Using Scientific Computational Package

Advances in semiconductor process technologies nowadays allow the realization of complex for modern Large Scale Integrates Circuits (LSIs). LSIs are moving towards the integration of systems on a single chip. These systems include both digital and analog elements on a single chip. For years almost of all designers have been using computer-aided design tools so as to cut total design time and costs and increase efficiency.

In the digital circuit design, it is possible to design composed of transistors as shown in Fig. 1.1 circuit included in the logic circuit to generate a complex logic circuit with their basic logic cells, such as AND or OR. Then in order to ensure that the circuit operates properly, it is needed that we estimate circuit delay, optimize delay, and confirm to be within a required delay.

As a method for calculating a signal delay, using the analytical expression simulation methodology and numerically solving the circuit equation in accordance with the category of the circuit, a method using a characteristic table that has been characterize advance. Among these techniques, the former method is accurate but not suitable for large circuits because of large time costs, so the latter method is generally used. As an application of the digital circuit design computer algebra system, it is possible to apply the method based formula using algebra system to delay estimation using the latter approach.

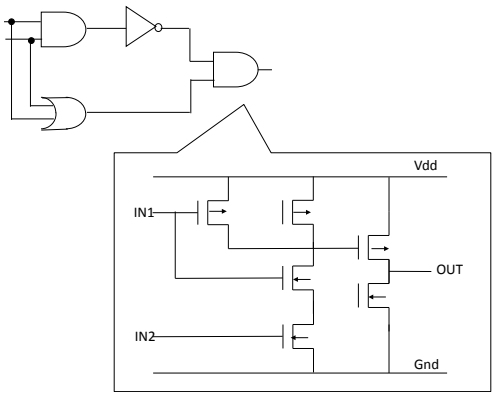

Figure 1.1: CMOS logic circuit and transistor components.

1.2 Equation-based Design and Analysis for Analog circuits

Next, we explain for the application of computer algebra systems to the analog circuit design. When designing linear circuit such as an amplifier which is typical analog circuit, we determine circuit topology first. The circuit structure means the way of connection of elements such as resistance, capacitance, transistor, etc. Based on the constraints and specifications, designers select the one from a lot of circuit structures. Then they determine parameter value, element size for each element of circuit structure that they have selected. They give appropriate initial values for each element parameter and get the final value by repeating the parameter adjustment and circuit simulation. It is very important to know that the initial value is appropriate to design values and which parameter is to affect the properties in order that it may be reduced design time and cost.

Now it is necessary to derive the characteristic equation for the topology so as to determine the sensitivity of the parameter and the initial value. Here, the characteristic equation is a mathematical equation that represents the characteristics of the circuits, it is represented by a

rational expression of the element parameters in general. At first, the designers perform a linear approximation of the circuit to a level which can calculate manually for the circuit topology they selected. Then they built a circuit equations based on the model, and derive the characteristic formula. They can calculate a reasonable advance an initial value from the characteristic expression. Further, it is possible to obtain simultaneously information of whether may be adjusted any parameter to change properties.

For the linear approximation of the circuit, professional know-how is required in order to model with clear parameters less affected. Since the quality of the model may greatly affect the subsequent processes, so that a good model fitting is required for the designers. In addition, as the number of parameters increases, characteristic equation is complicated exponentially. The more each characteristic equation becomes complicated, the more it becomes difficult to manually calculate the initial value of all the parameters and know the parameter sensitivity for each property.

We present that the symbolic computational method of analog circuit design and analysis is useful to reduce time and cost for manual calculation when the designer derive characteristic equation from circuit topology and calculate the initial parameter value from each characteristic equation.

1.3 Overview of this thesis

The objective of this research is to apply specifically the equation-based method using scientific computation package to the LSI circuit design.

This thesis is organized as follows. Chapter 2 focuses the application of the computer algebra approach to the design of integrated circuits, the estimation of signal delay or the thermal analytical modelling of interconnect for digital integrated circuits using Mathematica.

Chapter 3 discusses the symbolic method to the design of a power loop system. This is more complex than previously reported work and is particularly important in modern integrated circuit design. As a first step, we model an amplifier circuit and an LCR circuit using transfer functions. We also model an error detection and feedback loop. We then derive the transfer function of the entire power supply stabilization loop circuit by composing these functions. Finally, we chose a design target and determine the most suitable circuit parameters to satisfy it. To obtain these parameters, we solve a system of nonlinear equations using the symbolic algebraic manipulation functionality in Mathematica.

Chapter 4 and 5 describe numerical circuits Analysis with computer algebra system. Chapter 4 proposes a technique for simple electro-thermal equivalent circuit level modeling and reliability circuit simulation of power MOSFETs with SystemC-AMS/NGSPICE [11] [16]. As a case study, we focus on an Unclamped Inductive Switching (UIS) test circuit that is used for an avalanche breakdown test of MOSFETs. The avalanche breakdown is affected by device junction temperature rise that is due to self-heating of MOSFETs. In the reliability circuit simulation, it is essential that coupling of the electrical behaviour and thermal behaviour (electrical-thermal coupling) is considered [4] [9]-[10] [13] [14] [17]. The goal is to present an equation-based electro-thermal coupling modeling and transient (time domain) analysis of MOSFETs with Mathematica. In Chapter 5, we present a new technique of equation-based circuit design for DC/DC converters. We model the characteristics on frequency domain of a buck DC/DC converter with a loop compensation, and express as a transfer function. And we optimize efficiently design parameters of MLCC capacitor, which is a kind of output capacitors, in order to satisfy the circuit design specification. We implement the technique as an equation-based design program for buck DC/DC converters using Scilab. Our experimental results demonstrate that our technique has the capacity of dealing with the practical industrial design/analysis, and

its performance is superior to that of a power electronics circuit simulator.

Chapter 6 proposes a technique for large scale power grid analysis with a parallel computing method in Mathematica. We model a power grid as a system of ordinary differential equations, and apply the parallel computing method to get a solution efficiently. We explain the technique using a linear RC elements network model as the power grid. Our experimental results demonstrate that the technique is capable of the time domain analysis just the same as SPICE, a general-purpose circuit simulator, and is applicable to power grid design of LSI chips. And they reveal the superiority of our technique for the power grids of very large scale, and also indicate the effectiveness of the parallel computing method in the power grid optimization design.

Chapter 7 summarizes and concludes this dissertation.

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Chapter 2
Symbolic Circuits Analysis and Design with Computer Algebra System

2.1 CMOS Logic Circuits Design with Symbolic Computation

2.1.1 Introduction

In the digital circuit design, we need to estimate and optimize circuit delay in order to ensure that the circuit operates properly. With the scaling trend of feature sizes of manufacturing process and multilayer interconnect structure due to increase frequency and integration of LSI, parasitic capacitance and resistance of interconnect have a great impact on signal delay [1][2][4]. In general, there are some methods for calculating signal delay to be described below. The first is using the analytical simulation methodology or numerically solving the circuit equation in accordance with the category of the circuit. The second is using a characteristic table that has been characterized in advance. Among these techniques, the former method is accurate but not suitable for large circuits because of large time costs, so the latter method is generally used. As an application of the digital circuit design computer algebra system, we apply the method based formula using symbolic computation to delay estimation using the latter approach.

In other words, we propose a method of logic circuits delay analysis using non-linear delay model with symbolic computation. At first, we model a delay characteristic of basic cells by a mathematical representation of an approximate polynomial. Next, we design a 1-bit full adder circuit with our proposed method. As a result, we obtain the optimize design parameters with equation-based expression and we confirmed the usefulness of our proposed method.

2.1.2 CMOS Non-linear Delay Model

We consider how to achieve delay calculation of logic circuits by using non-linear delay models with symbolic computation.

Total delay of logic circuits, D_{total} is the sum of D_{cell} and $D_{interconnect}$ as shown in Fig. 2.1, where D_{cell} is typically defined as the 50 percent of input pin voltage to 50 percent of output voltage as shown in Fig. 2.2 and $D_{interconnect}$ is interconnect delay and D_{cell} is called cell or gate delay which is usually represented the function of both output load capacitance and input transition time [12].

Now we explain cell delay calculation method by using look up table which is characterized in advance and interpolation. Cell delay is obtained as follows by using a two-dimensional cell delay table that is used as an index of the input transition time and output load capacitance as shown in Fig. 2.3:

1) Determine output transition time and cell delay of cell U1 as an index the transition time at the previous cell U0 and output load capacitance of cell U1 from the delay table of cell U1.
2) Determine output transition time and cell delay of cell U2 as an index the transition time at the previous cell U1 which is obtained from 1) and output load capacitance of cell U2 from the delay table of cell U2.
3) Repeat the same operation later.

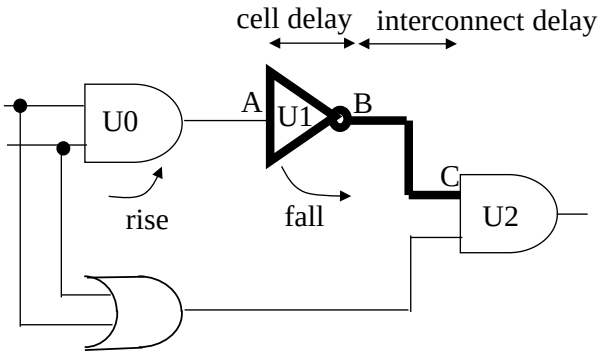


Figure 2.1: Components for CMOS non-linear delay model.

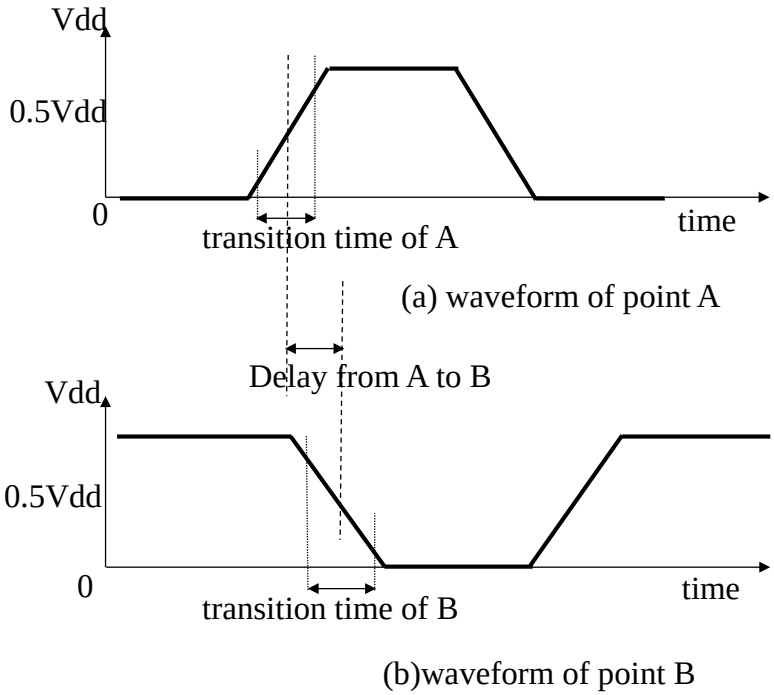


Figure 2.2: Definition of delay.

Here, to determine the cell delay from the cell delay table indexed by output load capacitance and input transition time, select the table value of four adjacent, including the index value at first. Next, determine the coefficient by the two-dimensional interpolation using the Gaussian elimination method in order to find an approximate value of the surface formed by the four points.

We show performing these calculations with example, output load capacitance to be α and the input transition time β. We can now index into U1's in Fig. 2.1 fall cell delay table with these two values. Four neighboring table values are determined by examination of the table breakpoints.

For example, the input transition time, α falls between the index values of T2 and T3. The output load capacitance β falls between the index values of C2 and C3. The index values correspond to the x and y coordinates of the four neighboring table points as shown in Fig. 2.3. The corresponding z values are also shown in Fig. 2.3.

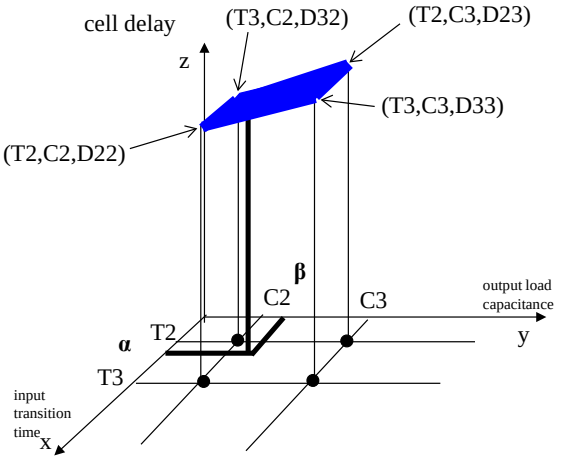
We determine the approximation for the surface described by the three coordinates (x, y, z) in Fig. 2.3 by solving the A, B, C, and D coefficients of the following equation. Next, insert the coefficient values into the equation to determine which z-coordinate relates to the fall cell delay.

$$Z = A + B \times x + C \times y + D \times x \times y$$

We can derive the coefficients A, B, C, and D with common mathematical method, such as Gaussian elimination method, as shown in following example.

$$D22 = A + B \times T2 + C \times C2 + D \times T2 \times C2$$
$$D23 = A + B \times T2 + C \times C3 + D \times T2 \times C3$$
$$D32 = A + B \times T3 + C \times C2 + D \times T3 \times C2$$
$$D33 = A + B \times T3 + C \times C3 + D \times T3 \times C3$$

Similarly, we can derive the coefficients for transition time with transition time table as shown in Fig. 2.3.



cell delay table

input transition time \ output load capacitance	C1	C2	C3	.....
T1	D11	D12	D13	
T2	D21	D22	D23	
T3	D31	D32	D33	
⋮				

transition time table

input transition time \ output load capacitance	C1	C2	C3	.....
T1	S11	S12	S13	
T2	S21	S22	S23	
T3	S31	S32	S33	
⋮				

Figure 2.3: Delay calculation and its table.

2.1.3 Modeling of the basic cell delay characteristic

For the cell delay table indexed by output load capacitance and input transition time described above, we consider that optimizes the coefficients to perform polynomial approximation using the least squares method and express by equation circuit delay characteristics. Here we consider fall delay of inverter cell as a basic cell. The cell delay table and transition time table are also given in the table of 7×7 which is indexed by output load capacitance and input transition time shown in Fig. 2.3. Then, we optimize the coefficients using a least squares method to the table, and express in the approximate polynomial from the first to sixth order. Fig.2.4 shows the RMS error for a two-dimensional table value and original number of terms.

Fig.2.5 plots the fall delay time of the cell to the output load capacitance and input transition time with respect to a polynomial approximation of the first degree, second degree, …, sixth degree. However, as can be seen from Fig. 2.4 and 2.5, it is high accuracy as well becomes higher degree, the polar is present when it is fourth or higher degree. To avoid this, we adopt the approximation by a cubic polynomial illustrated in Fig. 2.6.

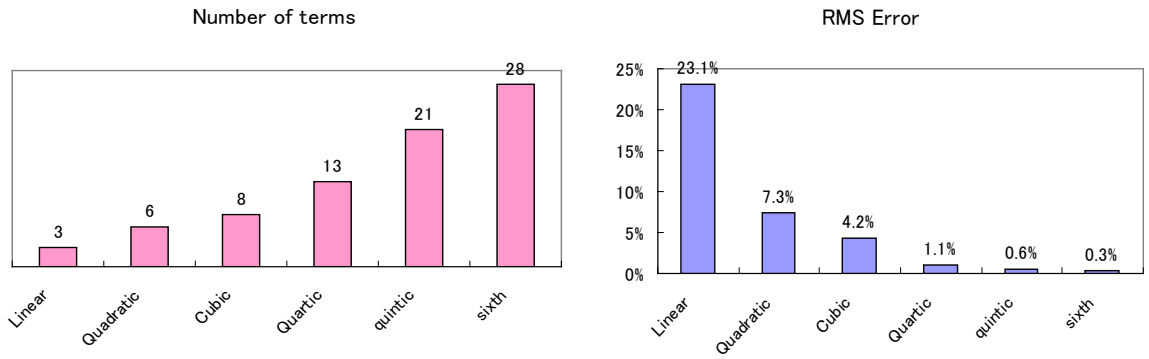


Figure 2.4: Number of terms and RMS error of the polynomial approximation.

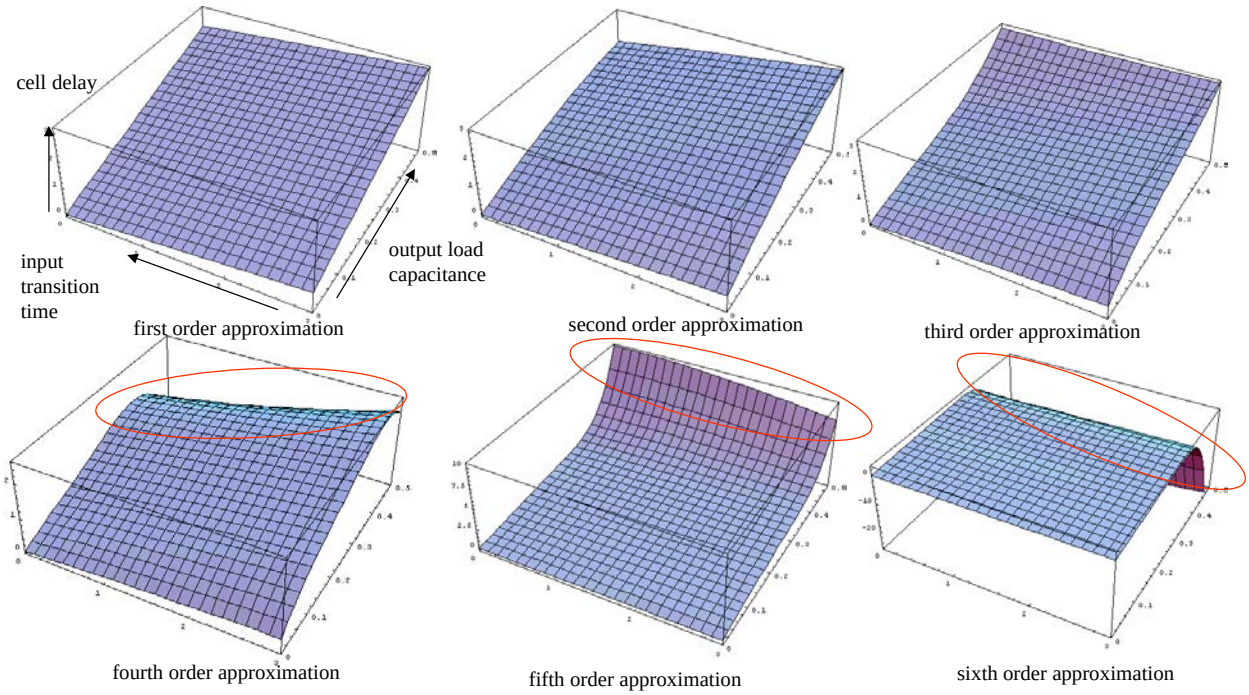


Figure 2.5: Example of the approximation of the inverter cell delay.

$$\begin{aligned}\text{INV\_fall}(x,y) = {} & -0.000986861 + 0.205682\,x - 0.0240294\,x^2 + 0.000884093\,x^3 + 5.7546\,y + \\ & 1.17031\,xy + 0.0900426\,x^2y - 11.6989\,y^2 - 3.32541\,xy^2 + 25.7925\,y^3\end{aligned}$$

x : input transition time
y : output load capacitance

Figure 2.6: Example of the approximation formula of the inverter cell delay.

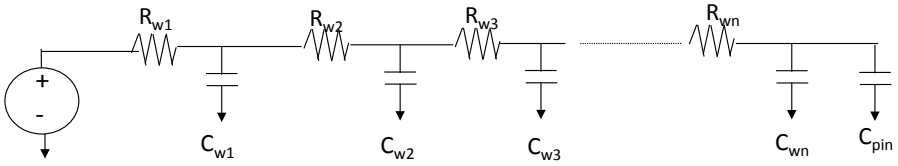
2.1.4 Design of 1bit Full Adder Circuit

2.1.4.1 Total Delay Calculation

As an application example to a real circuit, we design 1-bit full adder shown in Fig.2.8. Here, the parameters that we should obtain are interconnect length connecting between cells, L1, L2, L3, L4, L5 shown in Fig. 2.8. The design constraint is upper/lower limit of a delay from input A to output S and upper limit of output load capacitance of each cell. Then, transition time of input signal, so called Input slew and output load capacitance, so called Output load are given as specifications. Now we optimize each interconnect length for given Input slew and Output load.

Now we apply Elmore delay model [4] [6] shown in Fig. 2.8 as interconnect delay model. The calculation flow of total delay from input A to output S using symbolic computational system Mathematica is illustrated in Fig. 2.9. Now we model by approximate cubic polynomial whose parameters are the Output load and Input slew characteristic of each cell as described in the previous section. Here, Output load is the sum of interconnect capacitance and input capacitance of the next stage cell. In Fig. 2.9, *Dcellx* is delay of cell x and *DLYx* is its function, and *Tcellx* is output transition time and *Tcellx* is its function, further R0 (Ω/um) and C0 (F/um) is respectively interconnect resistance and capacitance per unit length that is obtained from manufacturing process.

We approximate total delay obtained in the present calculation flow by polynomial whose parameters are Input_slew, Output_load and interconnect length ($Length_1$,…, $Length_5$). As a result, we obtained 27th-degree approximation polynomial.



$D_{wire} = R_{w1}C_{w1}+(R_{w1}+R_{w2})*C_{w2}+\cdots(R_{w1}+R_{w2}+\cdots+R_{wn})*C_{wn}$

Especially, for all j, if $R_j=R$, $C_j=C$,

$$D_{wire} = RC * n(n+1) / 2$$

C_{pin} is obtained manufactualling process.
R_{wi} (i=1,…,n) is R_0 * wire length, where R_0 = sheet resistance / wire width.
C_{wi} (i=1,…,n) is C_0 * wire length.
And, we assume wire width is fixed in the design.

Figure 2.7: Interconnect model.

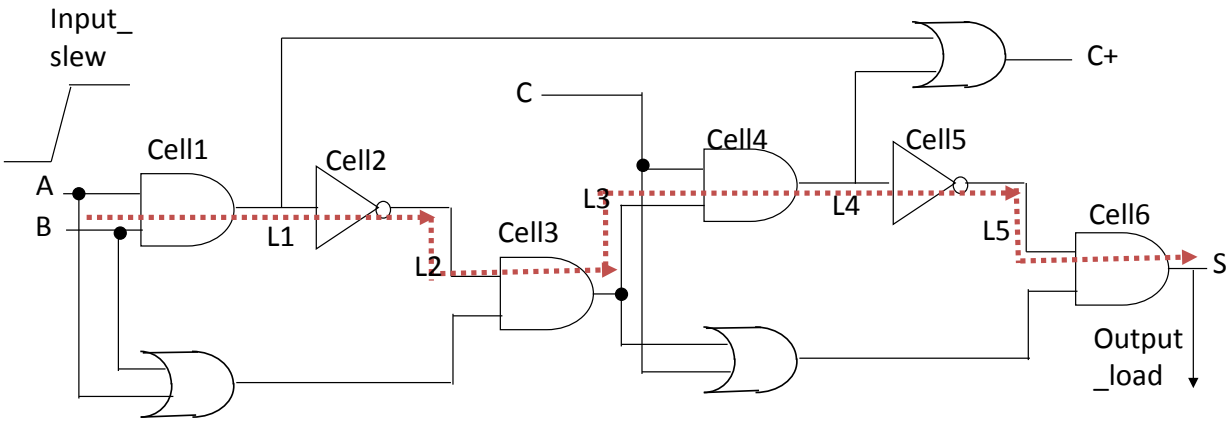


Figure 2.8: Schematic of 1bit full adder circuit.

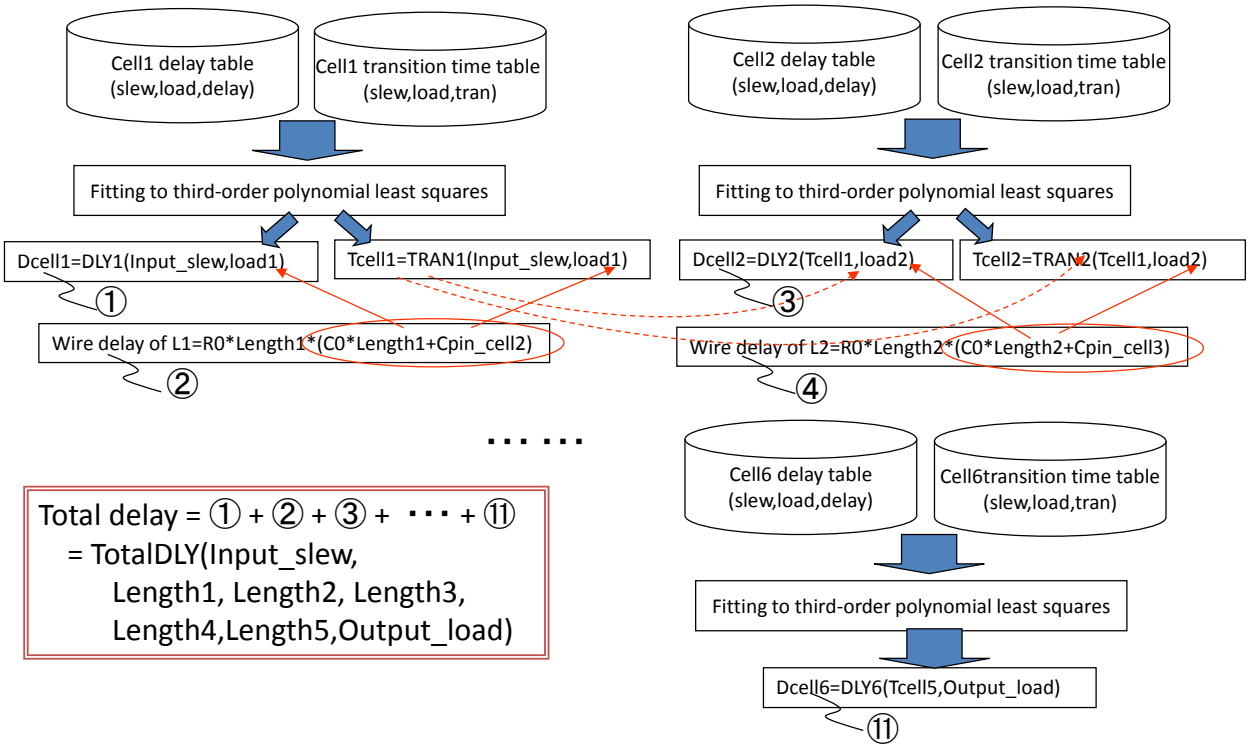


Figure 2.9: Calculation Flow.

2.1.4.2 Interconnect Length Optimization

The total delay determined previous section is represented by the function as parameter, Input_slew, Output_load and each interconnect length, $Length_1$, …, $Length_5$. Output load capacitance of each cell is sum of interconnect load capacitance that is C_0 (F/um) × interconnect length and input capacitance of next stage cell, C_{pin}. The constraint condition is described below:

(1) $D_{min} \leq$ Total delay $\leq D_{max}$
(2) $load_1 \leq C_{max1}$, $load_2 \leq C_{max2}$, $load_3 \leq C_{max3}$, $load_4 \leq C_{max4}$, $load_5 \leq Cmax_5$

where D_{min} , D_{max} are specification and $load_1$, …, $load_5$ are output load capacitance from $Cell_1$ to

$Cell_5$ and $Cmax_1$, … , $Cmax_5$ are constraint conditions from obtained manufacturing process.

Under the condition (1) and (2), we optimize interconnect length, $Length_1$, …, $Length_5$ for a combination of n Input_slew and Output_load given arbitrarily. As a result, we obtained Input_slew, Output_load and optimized interconnect table shown in Fig. 2.10. Then, we approximated interconnect length of $Length_1$,…, $Length_5$ from this interconnect length table by third-degree polynomial in order to model by the approximation polynomial equation whose parameters are Input_slew and Output_load shown in Fig. 2.11. Fig. 2.12. Then we shows RMS error of the approximation polynomial above to interconnect length table shown in Fig. 2.10. We found the RMS error is within 1%.

(Input_slew,Output_load,Length1,Length2,Length3,Length4,Length5)
$(s_1,O_1,Lo_{1\_1},Lo_{2\_1},Lo_{3\_1},Lo_{4\_1},Lo_{5\_1})$
$(s_2,O_2,Lo_{1\_2},Lo_{2\_2},Lo_{3\_2},Lo_{4\_2},Lo_{5\_2})$
$(s_3,O_3,Lo_{1\_3},Lo_{2\_3},Lo_{3\_3},Lo_{4\_3},Lo_{5\_3})$
:
:
$(s_n,O_n,Lo_{1\_n},Lo_{2\_n},Lo_{3\_n},Lo_{4\_n},Lo_{5\_n})$

Figure 2.10: Interconnect length table.

Length1= $56.2706 + 14.0774x - 25.6254x^2 + 12.6111x^3 + 352.036y - 46.557xy + 31.8844x^2y - 3466.32y^2 + 54.5149xy^2 + 5087.15y^3$

Length2= $166.617 + 65.6652x - 152.015x^2 + 93.0336x^3 + 180.61y + 706.275xy - 344.757x^2y - 3095.31y^2 - 1044.05xy^2 + 6243.48y^3$

Length3= $137.207 + 67.3216x - 204.595x^2 + 135.224x^3 - 1230.47y + 424.636xy - 205.38x^2y + 4804.82y^2 - 514.248xy^2 - 5743.89y^3$

Length4= $327.457 - 84.2874x + 223.271x^2 - 139.394x^3 + 735.468y - 901.97xy + 419.273x^2y - 2882.1y^2 + 1261.5xy^2 + 2311.37y^3$

Length5= $119.946 + 78.9733x - 240.862x^2 + 152.843x^3 - 2839.19y + 1401.86xy - 638.947x^2y + 17538.3y^2 - 1942.6xy^2 - 24435.2y^3$

Figure 2.11: Optimization result.

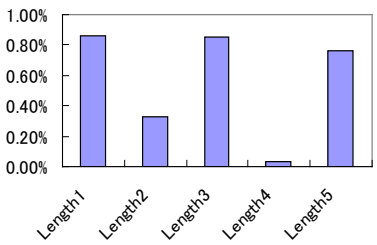


Figure 2.12: RMS error.

2.1.5 Conclusion

We proposed delay calculation method of CMOS logic circuit by using symbolic computation. We first modeled delay characteristic of basic cell by third-order polynomial expression. The accuracy was 4.2%. Further we designed 1-bit full adder circuit by using proposed method. Then we approximated delay characteristic of this circuit by 27-order polynomial and optimized interconnect length by third-order polynomial. Thus, we showed proposed method by symbolic computation is useful for delay calculation.

2.2 Thermal Analysis for LSI with Symbolic Computation

2.2.1 Introduction

In the manufacturing process, the size of multilayer interconnect structure becomes finer and finer, due to the frequency increase and integration of LSI. So, a new problem becomes critical. As an immediate problem, there is a self-heating problem with increasing the current density of LSI interconnects. As the temperature of interconnect increases, the circuit performance reduces.

For this problem, the thermal analysis must be considered in each level of system design, architecture design and physical design [7]. But most of current commercial CAD tools do not consider the thermal analysis seriously. The objective of our research is to apply symbolic estimation to analysis of self-heating in interconnects and then estimate easily and precisely signal delay considering temperature dependence. Furthermore, we construct a tool for signal delay calculation tool considered temperature dependence of interconnect.

2.2.2 Motivation

Consider distributed RC model of interconnect shown in Fig. 2.13. Using the general Elmore delay model [9], signal delay "*D*" from driver input to receiver input of next stage is expressed as Eq. (2.1).

$$D = R_d((\sum_{i=1}^{n} c_0(x_i) \bullet \Delta x) + C_d + C_L) + \sum_{i=1}^{n} r_0(x_i) \bullet \Delta x \bullet (\sum_{j=1}^{n} c_0(x_j) \bullet \Delta x + C_L) \quad (2.1)$$

where r_0 is interconnect resistance per unit length, c_0 is interconnect capacitance per unit length, and C_L is receiver input pin capacitance of next stage.

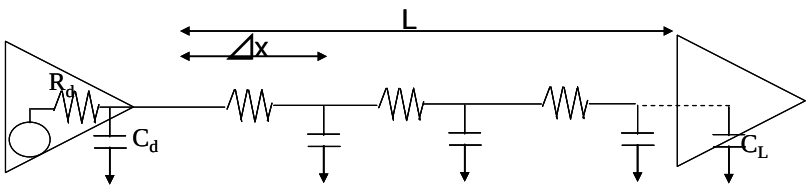


Figure 2.13: Elmore delay model.

In Fig. 2.13, if it is assumed that there are infinite RC ladder split, Eq. (2.1) is expressed by Eq. (2.2).

$$D = R_d(C_d + C_L + \int_0^L c_0(x)dx) + \int_0^L r_0(x) \bullet (\int_x^L c_0(\tau)d\tau + C_L)dx \quad (2.2)$$

On the other hand, a relation between interconnect resistance "R" and temperature "T" is generally approximated by Eq. (2.3)

$$R = R_0(1 + \alpha(T - T_0)) \quad (2.3)$$

where T is analyzing temperature, T_0 is reference temperature, R_0 is resistance when temperature is T_0, and α is temperature coefficient of interconnect. Then, α is equal to about 0.003 in case of copper interconnect being used in semiconductor manufacturing. Fig.2.14 shows temperature dependence of the interconnect resistance using Eq. (2.2). As shown in Fig. 2.14 and Eq. (2.2), if the interconnect temperature is 100℃ rise, the interconnect resistance increases about 30%. As interconnect resistance increase, interconnect delay is increased expressed in Eq. (2.2).

Now we can describe Elmore delay model in Eq. (2.2) as Eq. (2.4), under considering of the temperature dependence of the interconnect resistance of Eq. (2.3).

$$D = D_0 + (c_0 L + C_L)r_0\alpha\int_0^L T(x)dx - c_0 r_0 \alpha \int_0^L x \bullet T(x)dx \quad (2.4)$$

where D_0 is delay at reference temperature as below.

$$D_0 = R_d(C_L + c_0 L) + (c_0 r_0 \frac{L^2}{2} + r_0 L C_L) \quad (2.5)$$

Fig.2.15 shows that temperature of LSI interconnect impacts on interconnect delay. The X axis is temperature, and the Y axis is relative value the delay considered temperature dependent for not considered it. The reference temperature is assumed 25℃. If the Y axis is plus, our delay estimation is overestimate than actual delay. And if it is minus, our estimation is underestimate.

Also, Fig.2.15 indicates that when not considering interconnect temperature, as the temperature increase, delay estimation become underestimate. Conversely as the temperature decrease, delay estimation become overestimate. For example, the temperature reaches 125℃ from 25℃, the rate of change of interconnect delay 15%. And the temperature reaches -40℃ from 25℃, the rate of change of interconnect delay 15%. Therefore, we find that the accurate delay estimation considered interconnect temperature change is required to signal delay calculation.

In next section, we do thermal analysis of one-dimensional steady-state of LSI interconnect from the basic equation of heat conduction using equation based computation and consider its modeling.

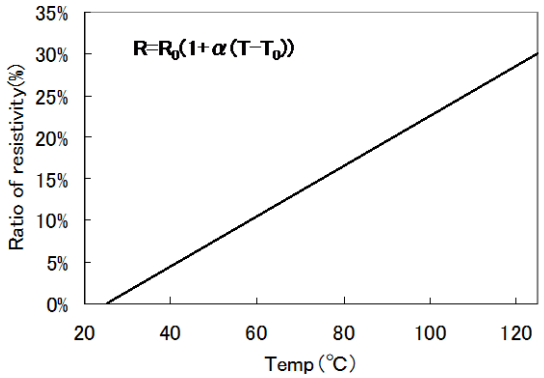


Figure 2.14: Interconnect resistance dependence on temperature.

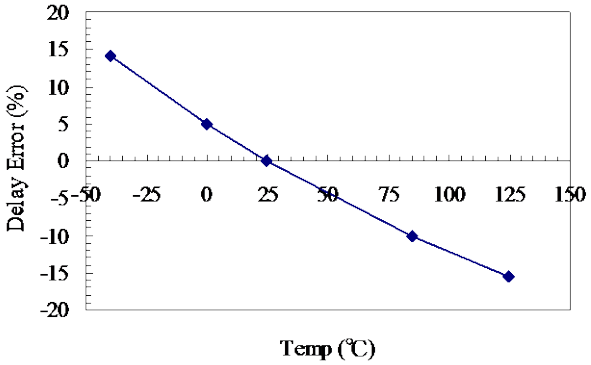


Figure 2.15: Interconnect temperature impact on delay.

2.2.3 Thermal Analysis for LSI Interconnect

2.2.3.1 Heat Conduction Model

Thermal conductivity of the 3-dimensional object inside is expressed by partial differential equations below.

$$\frac{\partial}{\partial x}(k\frac{\partial T}{\partial x})+\frac{\partial}{\partial y}(k\frac{\partial T}{\partial y})+\frac{\partial}{\partial z}(k\frac{\partial T}{\partial z})+Q^{*}=c\rho\frac{\partial T}{\partial \tau} \tag{2.6}$$

where τ is time and T is temperature. And we represent by $Q^{*}(x,y,z,\tau)$ the internal heat generation per unit time and volume. Further c is specific heat, ρ is the density, and k is the thermal conductivity. Especially, the heat generation is steady-state, the left-hand side of Eq. (2.6) is 0.

2.2.3.2 Thermal Analysis Model of the LSI interconnect

In our research, we consider the thermal analysis method. Here the heat source is the power consumption of LSI interconnect. Fig.2.16 shows the LSI interconnect structure. In order to apply the thermal analysis of LSI interconnect shown in Fig.2.16 to heat conduction model described in previous section, we abbreviated to one-dimensional steady-state. Then we can represent the heat conduction equation as Eq. (2.7).

$$\frac{d^{2}T}{dx^{2}}=-\frac{Q^{*}}{k_{m}} \tag{2.7}$$

where k_m is the thermal conductivity of LSI interconnect.

Now in Fig.2.16, assuming that P_g power consumption of LSI interconnect, the power consumption $P_g(x)$ of the small interval for the interconnect length is expressed as follows.

$$P_g(x) = I_{rms}^2 \Delta R_E(x) \tag{2.8}$$

where I_{rms} indicates root mean square of the current passing through the interconnect, and R_E is the electrical resistance of interconnect.

If the interconnect temperature is changed, the temperature difference is generated in the substrate directly under interconnect and itself. When the reference temperature to the temperature of the substrate immediately below interconnect, the interconnect resistance R_0 at the reference temperature is given by the following equation Eq. (2.9).

$$\Delta R_0(x) = \rho_l \frac{\Delta x}{w t_m} \tag{2.9}$$

where ρ_l is electrical resistivity of the interconnect at the reference temperature, t_m is interconnect thickness, and w is interconnect width.

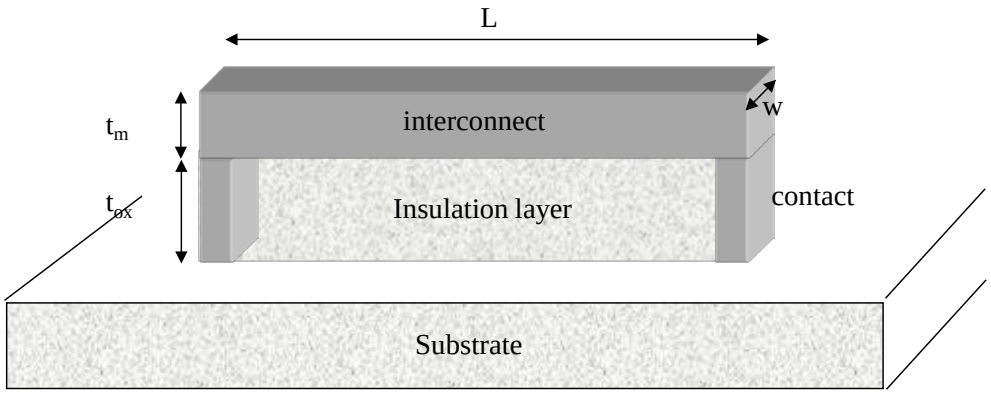


Figure 2.16: Interconnect structure.

On the other hand, emission of thermal energy $P_l(x)$ by heat transfer as the current passes through the insulation layer between the substrate and the interconnect can be expressed by the following equation Eq. (2.10) in the section Δx.

$$P_l(x) = \frac{T_{line}(x) - T_{ref}(x)}{\Delta R_T(x)} \tag{2.10}$$

where

$$\Delta R_T(x) = \frac{t_{ox}}{k_{ox} w_{eff} \Delta x} \tag{2.11}$$

and T_{line} is interconnect temperature, T_{ref} is reference temperature, temperature of the substrate interconnect directly under, R_T is thermal resistance of insulation layer, k_{ox} is thermal conductivity of insulation layer, t_{ox} is thickness of insulation layer, w_{eff} is effective interconnect width in the case of considering the fringe effect of the interconnect side that is approximated $w(1+0.88t_{ox}/w)$ [10].

From the above, thermal energy generation amount of interconnect per unit volume is

$$Q^* = \frac{P_g - P_l}{wt_m \Delta x} \tag{2.12}$$

Therefore using the one-dimensional heat conduction equation expressed in Eq. (2.7) in the steady-state, the heat diffusion equation of interconnect structure shown in Fig. 2.16 is obtained.

$$\frac{d^2 T_{line}(x)}{dx^2} = \lambda T_{line}(x) - \lambda T_{ref}(x) - \theta \tag{2.13}$$

where,

$$\lambda = \frac{l}{k_m}\left(\frac{k_{ox}}{t_m t_{ox}}\left[1 + 0.88\frac{t_{ox}}{w}\right] - \frac{I_{rms}^2 \rho_l \alpha}{w^2 t_m^2}\right) \tag{2.14}$$

$$\theta = \frac{I_{rms}^2 \rho_l}{w^2 t_m^2 k_m} \tag{2.15}$$

where λ and θ is a constant that depends on the interconnect structure and technology.

Now, the thermal resistance of the substrate contact is very small, so we can be considered that the temperature of both ends of the longitudinal direction of the interconnect is equal to the temperature of the substrate. And the surface temperature T_{ref} varies depending on the location because it depends on the probability of each switching cell, but we assume to be constant in this case. That is, the temperature at both ends of interconnect can be expressed by Eq. (2.16).

$$T(x=0) = T_{ref}, T(x=L) = T_{ref} \tag{2.16}$$

2.2.3.3 One-dimensional Numerical Simulation

We solve one-dimensional linear equation represented by Eq. (2.13) using difference solution under the boundary condition Eq. (2.16). Before solving Eq. (2.13), we first consider a boundary value problem of the one-dimensional linear equations.

$$u'' = p(x)u'(x) + q(x)u(x) + r(x) \tag{2.17}$$
$$\text{Boundary condition}: u(x_0) = \alpha, u(x_n) = \beta$$

where p, q, r are given functions, and α, β are given constants. Using n number of equinox x_j (j=1,2,…,n), we divide a section $x_0 \le x \le x_n$ to small section [x_j,x_{j+1}] which length h is (x_n-x_0)/(n+1) as shown in Fig.2.17.

where $x_0 < x_1 < x_2 \cdots < x_n$.

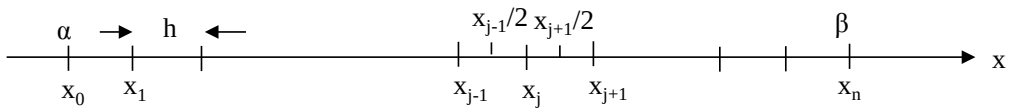


Figure 2.17: Equinox of one-dimensional finite difference method.

We approximate unknown function *u(x)* in Eq. (2.17) by using values that are defined in the equinox. Then the central difference approximation first derivative and the second derivative is as follows.

$$u'(x_j) = \frac{u(x_{j+1}) - u(x_{j-1})}{2h} + O(h^2) \tag{2.18}$$

$$u''(x_j) = \frac{u(x_{j+1}) - 2u(x_j) + u(x_{j-1})}{h^2} + O(h^2) \tag{2.19}$$

We represent the term $u(x_j)$ of the right side in Eq. (2.18) and Eq. (2.19) by u_j and approximate by a second order of h. Further by expressing $p_j=p(x_j)$、$q_j=q(x_j)$、$r_j=r(x_j)$, we obtain the following difference equation Eq. (2.20).

$$\frac{u_{j+1} - 2u_j + u_{j-1}}{h^2} = p_j \frac{u_{j+1} - u_{j-1}}{2h} + q_j u_j + r_j \tag{2.20}$$

Then rearranging Eq. (2.20), we obtain Eq. (2.21).

$$\begin{gathered}(-\frac{h}{2}p_j - 1)x_{j-1} + (2 + h^2 q_j)x_j + (\frac{h}{2}p_j - 1)x_{j+1} = -h^2 r_j \\ j = 1,2,\cdots,n-1,\ \ u_0 = \alpha,\ u_n = \beta\end{gathered} \tag{2.21}$$

Making a formula Eq. (2.21) for each j, and given the boundary value, simultaneous linear equations with coefficient matrix to tridiagonal matrix is obtained. Then we calculated using Mathematica [8] a system of linear equations with coefficient matrix to tridiagonal matrix.

2.2.4 Simulation Result

Fig. 2.18 shows our thermal simulation result of one-dimensional for structure in Fig. 2.16 using Mathematica [8]. It is the result when interconnect length is 100μm, 200μm, 500μm. Here, we used technology parameters used in the simulation as shown in Table 2.1, the value of 0.25μm equality ITRS [9] compliant.

In addition, we compared of the technology of 0.25μm and 0.1μm for the case that the interconnect length is 200μm, for the sake of knowing technology node dependence of one-dimensional heat distribution, seeing in Fig.2.19. We found that as technology become small, the maximum temperature of the interconnect increases, so the difference between the substrate become critical problem.

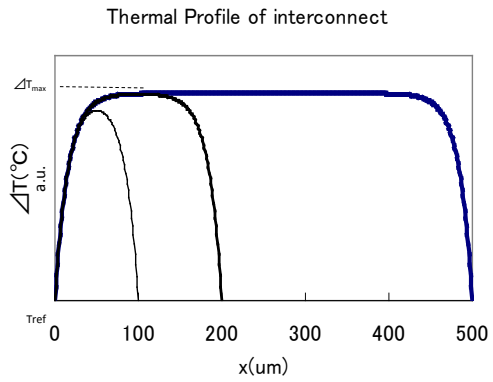


Figure 2.18: Thermal simulation result.

Table 2.1: Parameters value.

parameter	value	unit
k_m	4.0e-4	W/(um·K)
k_{ox}	4.0e-7	W/(um·K)
ρ_l	1.68e-2	Ω·um
β	3.0e-3	1/K
I_{rms}	2.0e-3	A
t_m,t_{ox},w	referenced 0.25um technology of ITRS*	

*) ITRS: International technology roadmap of semiconductor.

2.2.5 Polynomial Approximation

We consider to approximate by a polynomial one-dimensional thermal distribution in order to estimate the impact on delay from our simulation results. In Fig.2.20, we show the result of fourth-order and sixth-order and eighth-order polynomial approximation in case that the interconnect length is 200μm and 500μm. Further, Table 2.2 indicates the error for numerical solution. Here the error is represented by the sum of average and standard deviation.

From these results, as order become high, the accuracy of polynomial approximation is improved. But considering the trade-off accuracy and computational cost, when we assume that precision tolerance is within 5%, sixth-order polynomial approximation is most appropriate.

Next, we approximated by a polynomial of L coefficients of sixth-order polynomial in x in order to generalize the temperature at position x of interconnect which length is L. We show the approximated equation in Eq. (2.22). The error of our approximation is 4.7%.

$$T(x,L) = T_{ref} + f_0(L) + f_1(L)x + f_2(L)x^2 + f_3(L)x^3 + f_4(L)x^4 + f_5(L)x^5 + f_6(L)x^6 \quad (2.22)$$

where T_{ref} is the reference temperature and

$$f_0(L) = 8\times10^{-6}L^2 - 6\times10^{-4}L - 0.0313$$
$$f_1(L) = -4\times10^{-7}L^2 - 5\times10^{-4}L + 0.7001$$
$$f_2(L) = -4\times10^{-8}L^2 - 6\times10^{-5}L - 0.0258$$
$$f_3(L) = 2\times10^{-9}L^2 - 2\times10^{-6}L + 6\times10^{-4}$$
$$f_4(L) = -3\times10^{-16}L^4 + 5\times10^{-13}L^3 - 3\times10^{-10}L^2 9\times10^{-8}L - 1\times10^{-5}$$
$$f_5(L) = 6\times10^{-18}L^4 - 8\times10^{-15}L^3 + 5\times10^{-12}L^2 - 1\times10^{-9}L + 1\times10^{-7}$$
$$f_6(L) = -3\times10^{-12}L^4 + 4\times10^{-17}L^3 - 2\times10^{-14}L^2 + 5\times10^{-12}L - 4\times10^{-10}$$

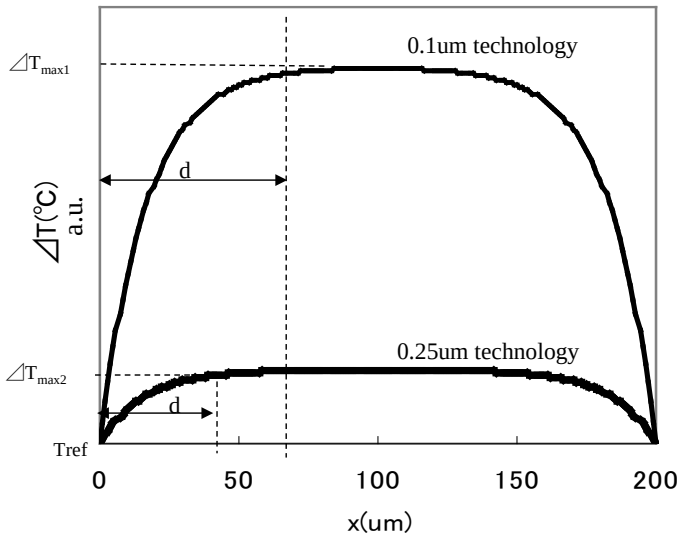


Figure 2.19: Polynomial approximation result.

Table 2.2: The error for numerical solution.

Degree of polynomial	L=200um	L=500um
4	12.9%	13.8%
6	1.5%	4.7%
8	0.3%	1.5%

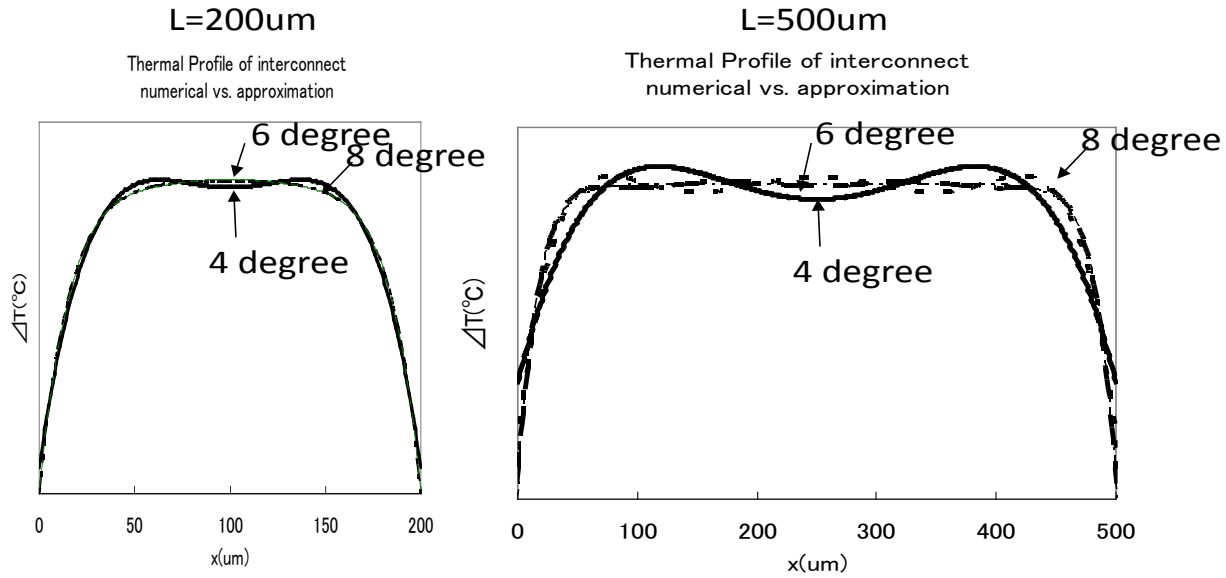


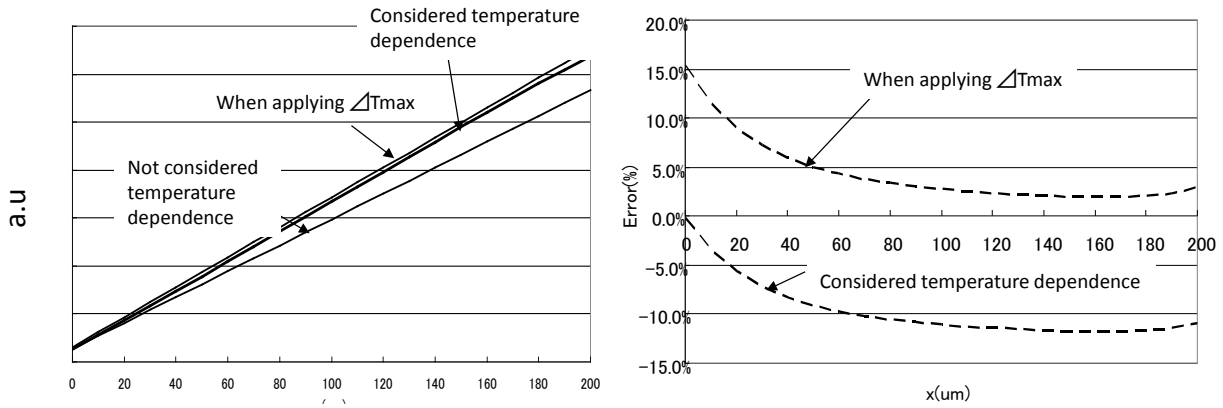
Figure 2.20: Polynomial approximation result in case that interconnect length is 200μm and 500μm.

2.2.6 Estimation of Impact on the Delay

Fig.2.21 shows the results of the Elmore delay equation taking into account the temperature dependence derived in Eq. (2.4), to determine the delay by substituting the approximate polynomial in temperature approximated above. In Fig.2.21, Fig.2.21 (a) represents a comparison of the delay time of the case of considered temperature dependence and not considered temperature dependence, and applying max temperature, $\triangle T_{max}$. And Fig.2.21 (b) represents an error in the case of not considering the temperature dependence and applying max

temperature ΔT_{max} for the case of considering it.

From this result, we obtain that maximum delay error is -10.9% in the case of not considering the temperature dependence, and maximum delay error is 15.3% if assuming that interconnect temperature is uniform.



(b) Comparison of delay. (a) Delay error.

Figure 2.21: Comparison of considering and not considering temperature.

2.2.7 Conclusion

We presented thermal analytical models of LSI by using symbolic computation. We provided the modeling of Joule heating in LSI interconnect under steady-state condition and show that the thermal profile of LSI interconnects is approximated by using polynomial representation. In addition, we estimated accurate and realistic signal delay by considering that interconnect resistance is dependent on the temperature. The results demonstrate good agreement with experimental data. Finally, thermal effects due to Joule heating in LSI interconnect on delay are found to be significant and the usefulness of our modeling is discussed.

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Chapter 3
Symbolic Computation to Design of a Power Supply Stabilization Loop Circuit

3.1 Introduction

As the first step, we model an amplifier circuit and an LCR circuit using transfer functions. We also model error detection and the feedback loop. Next we derive transfer function of the entire power supply stabilization loop circuit by composing the transfer functions of aforementioned circuit models. Finally, we chose a design target and determined the most suitable circuit parameters to satisfy it. To obtain the suitable values of these parameters, we solve a system of nonlinear equations using the symbolic algebraic manipulation functionality in Mathematica [6].

If we solve the system of nonlinear equations, we were unable to find a set of constants of circuit elements applicable to the target design. However, if we apply a symbolic algebraic technique to those nonlinear equations, we were able to obtain plural solutions. In addition, we found that each of the solutions had important meaning as a circuit parameter that constructed whole system. Next, we discuss how to symbolically solve nonlinear equations and what solutions can be obtained. In this way, we propose our practical symbolic technique for a power supply stabilization loop circuit.

3.2 The General Approach

One of the principal issues in analog circuit design is to find the most suitable circuit parameters using a transfer function that satisfies previously given specifications. In general, the network functions for analog circuits are rational functions (ratio of two polynomials) in the complex frequency variable *s* [3][4]:

$$\begin{aligned} \mathrm{H(s)} &= \frac{P(s)}{Q(s)} \\ &= \frac{a_0 s^n + a_1 s^{n-1} + \cdots a_{n-1} s + a_n}{b_0 s^m + b s^{m-1} + \cdots b_{m-1} s + b_m} \end{aligned} \tag{3.1}$$

where the numbers *m*, *n* and the coefficients $a_i\ (0 \le i \le n)$, $b_j\ (0 \le j \le m)$ are determined by the given specifications and both polynomial numerator and denominator are symbolic polynomial functions being represented by a symbol instead of a numerical value. The following example leads us to the various definitions of the symbolization. The circuit elements represented by symbols are distinguished in accordance with given or determined parameters [1] [2]:

Full symbolic network function:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + RCs + LCs^2} \tag{3.2}$$

Partially symbolic and partially numerical network function when C=50pF, L=600uH:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + 5.0e - 11Rs + 3.0e - 11s^2} \tag{3.3}$$

Now, in order to determine a target analog circuit, each element shown earlier is described by the following network function

$$\mathrm{T(s)} = \frac{\sum_{\mu=0}^{n} A_\mu(p_1, \cdots, p_k)s^\mu}{\sum_{\tau=0}^{m} B_\tau(p_1, \cdots, p_k)s^\tau} \tag{3.4}$$

where the terms A_μ and B_τ are polynomials in $p_1, \cdots, p_k$, and which satisfies

$$\mathrm{H(s)} = \mathrm{T(s)} \tag{3.5}$$

To solve the nonlinear simultaneous Eq. (3.5), we try to apply symbolic and numerical analysis, and confirm that the symbolic analysis results in suitable design solutions but numerical analysis does not.

3.3 Modeling of the system

Consider a power loop system as depicted in Fig. 3.1, which is composed of three sub blocks - block1, block2 and block3 indicated by dotted line.

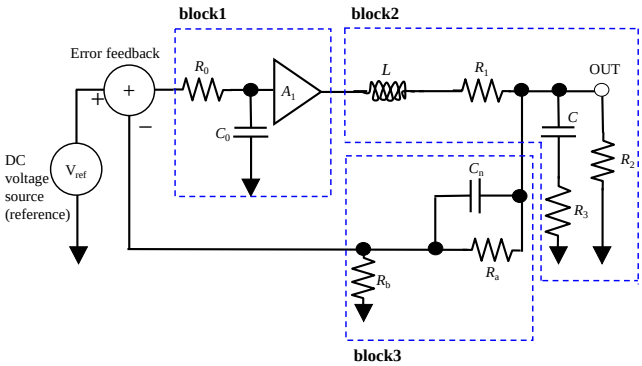
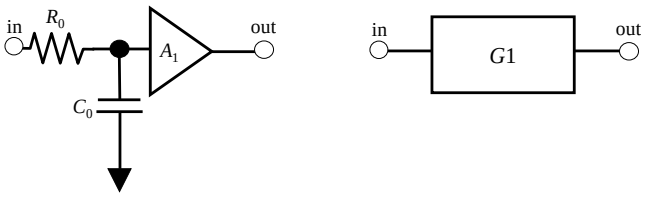


Figure3.1: A Power Loop System.

3.3.1 Modeling of block1

Block1 shown in Fig. 3.1 is an amplifier circuit. Fig. 3.2 shows the circuit and its transfer function.



(a)An amplifier circuit model (b) Transfer function of (a)

Figure 3.2: Model and transfer function of block1.

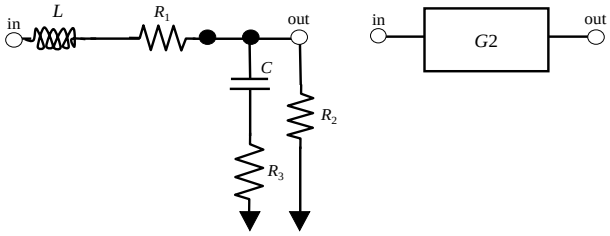
We see that the symbolic transfer function G1(s) of this circuit is given by:

$$\omega_1 = 1/(R_0C_0) = 2\pi f_1$$
$$G1(s) = \left(\frac{1/sC_0}{R_0 + 1/sC_0}\right)A_1 = \left(\frac{1/sR_0C_0}{1 + 1/sR_0C_0}\right)A_1 = \left(\frac{1/R_0C_0}{s + 1/R_0C_0}\right)A_1 = \left(\frac{\omega_1}{s+\omega_1}\right)A_1 \quad (3.6)$$

Note that f_1 is the frequency, and we are going to set its value later.

3.3.2 Modeling of block2

Block2 in Fig. 3.1 is a well-known LCR circuit. This circuit and its transfer function are shown in Fig. 3.3.



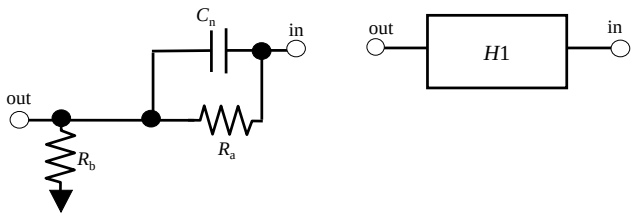
(a) LCR circuit model (b) Transfer function
Figure 3.3: Model and transfer function of block2.

We derive the symbolic transfer function G2(s) of this circuit as follows:

$$G2(s) = \frac{\left(R_3 + 1/sC\right)R_2}{\left\{R_1 + sL + \frac{R_2R_3}{\left(R_3 + R_2 + 1/sC\right)} + \frac{R_2}{sC\left(R_3 + R_2 + 1/sC\right)}\right\}\left(R_3 + R_2 + 1/sC\right)} \quad (3.7)$$

3.3.3 Modeling of block3

Finally, block3 shown in Fig. 3.4 is a feedback circuit as we know.



(a) Feedback circuit model (b) Transfer function
Figure 3.4: Model and transfer function of block3.

We derive the symbolic transfer function H1(s) of this circuit:

$$H1(s) = \frac{R_b}{R_b + \left(\frac{R_a \,/\, sC_n}{R_a + 1/sC_n} \right)} = \frac{R_b}{R_b + \left(\frac{R_a}{1 + sR_aC_n} \right)} \tag{3.8}$$

3.3.4 Modeling of the Full System

Now we are able to obtain the transfer function of the full system, constructed from block1, block2 and block3 as shown in Fig. 3.1. As we illustrate in Fig. 3.5, the full system has three linked transfer functions G1, G2 and H1.

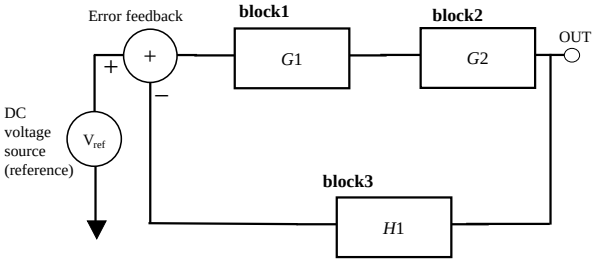


Figure 3.5: Transfer function model of our system.

In order to obtain the symbolic transfer function of the full systems, with using the symbolic computation package Mathematica 8 [6], we connect G1 and G2 via the "SystemModelSeriesConnect" command and then connecting it to H1 with the "SystemModelFeedbackConnect" command. As result, we find that the system symbolic transfer function is given by

$$T_{sys} = \frac{U_2 s^2 + U_1 s + U_0}{D_4 s^4 + D_3 s^3 + D_2 s^2 + D_1 s + D_0} \tag{3.9}$$

Where

$$\begin{aligned}
U_0 &= A_1\omega_1 R_2 R_a + A_1\omega_1 R_2 R_b\,,\\
U_1 &= A_1 C\omega_1 R_2 R_3 R_a + A_1 C\omega_1 R_2 R_3 R_b + A_1 C_n\omega_1 R_2 R_a R_b\ ,\\
U_2 &= A_1 C C_n\omega_1 R_2 R_3 R_a R_b\ \ ,\\
D_0 &= L\omega_1 R_a + \omega_1 R_2 R_a + \omega_1 R_1 R_b + \omega_1 R_2 R_b + A_1\omega_1 R_2 R_b\ ,\\
D_1 &= L\omega_1 R_a + R_1 R_a + R_2 R_a + C\omega_1 R_1 R_2 R_a + C\omega_1 R_1 R_3 R_a +\\
&\quad C\omega_1 R_2 R_3 R_a + L\omega_1 R_b + R_1 R_b + R_2 R_b + C\omega_1 R_1 R_2 R_b +\\
&\quad C\omega_1 R_1 R_3 R_b + C\omega_1 R_2 R_3 R_b + A_1\omega_1 R_2 R_3 R_b +\\
&\quad C\omega_1 R_1 R_a R_b + C_n\omega_1 R_2 R_a R_b + A_1 C_n\omega_1 R_2 R_a R_b\ ,\\
D_2 &= LR_a + CL\omega_1 R_2 R_a + CR_1 R_2 R_a + CL\omega_1 R_3 R_a +\\
&\quad CR_1 R_3 R_a + CR_2 R_3 R_a + LR_b + CL\omega_1 R_2 R_b + CR_1 R_2 R_b \quad +\\
&\quad CL\omega_1 R_3 R_b + CR_1 R_3 R_a + CR_2 R_3 R_a + C_n L\omega_1 R_a R_b +\\
&\quad C_n R_1 R_a R_b + C_n R_2 R_a R_b + CC_n\omega_1 R_1 R_2 R_a R_b +\\
&\quad CC_n\omega_1 R_1 R_3 R_a R_b + CC_n\omega_1 R_2 R_3 R_a R_b + A_1 CC_n\omega_1 R_2 R_3 R_a R_b\ ,\\
D_3 &= CLR_2 R_a + CLR_3 R_a + CLR_2 R_b + CLR_3 R_b +\\
&\quad C_n LR_a R_b + CC_n L\omega_1 R_2 R_a R_b + CC_n R_1 R_2 R_a R_b +\\
&\quad CC_n L\omega_1 R_3 R_a R_b + CC_n R_1 R_3 R_a R_b + CC_n R_2 R_3 R_a R_b\\
D_4 &= CC_n LR_2 R_a R_b + CC_n LR_3 R_a R_b\ .
\end{aligned} \tag{3.10}$$

We know some parameters in the previously given performance specification of the design, so we set A_1=60 (dB), and L=10 (μH). Also, we assume f_1=1(Hz), so $\omega_1 = 2\pi f_1 = 2\pi$. As result, Eq. (10) has seven unknown parameters. It is well-known that, it is difficult to obtain numerical solutions with Newton-Raphson approximation methods for nonlinear simultaneous equations.

3.4 Analysis and results

Then we try to perform the design task. To stabilize the power supply loop circuit, we set the following design target: a large enough phase margin and a gain margin of about 20 (dB) as shown in Fig. 3.6. We set the following transfer function (Eq. (3.11)) used in the industrial design settings as our design target.

$$Fsys = \frac{6000000(s+1000000)}{s^3 + 50000s^2 + 1000000000s + 3000000000000} \tag{3.11}$$

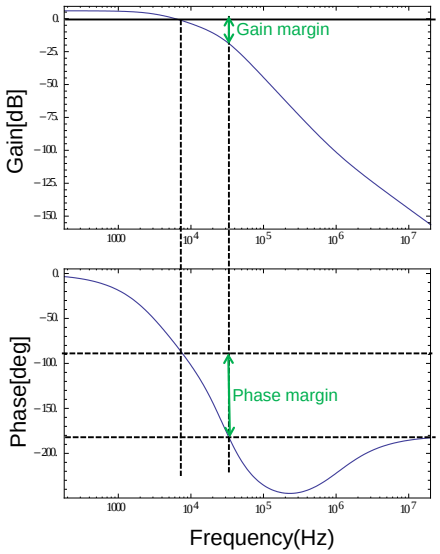


Figure 3.6: Bode Plot of the design target (Eq. (3.11)) .

When we assume T_{sys} = F_{sys}, we obtain the following equation.

$$\begin{aligned}&(U_2 s^2 + U_1 s + U_0)(s^3 + 50000s^2 + 1000000000s + 3000000000000) \\ &- 6000000(D_4 s^4 + D_3 s^3 + D_2 s^2 + D_1 s + D_0)(s + 1000000) = 0\end{aligned} \tag{3.12}$$

Factoring out common terms, we are left with a fifth order polynomial in s with coefficients being integer polynomials in the variables { R_1,R_2,R_3,R_a,R_b,C_n,C }. To solve Eq. (3.12), we need to set the coefficients to zero, then consequently we describe the set of Eq. (3.13):

$$\begin{aligned}0 \; = \; & 37680000000000 R_1 R_a - 18802320000000000 R_2 \\ & + 37680000000000 R_1 R_b + 18877680000000000 R_2 \, R_b\end{aligned}$$

$$
\begin{aligned}
0 \;=\; & 376800000R_a + 6000037680000R_1R_a - 279962320000R_2R_a \\
& +37680000000000CR_1R_2R_a + 37680000000000CR_1R_3R_a \\
& -18802320000000000CR_2R_3R_a + 376800000R_b \\
& +6000037680000R_1R_b - 242282320000R_2R_b \\
& +37680000000000CR_1R_2R_b + 18877680000000000CR_2\,R_3R_b \\
& +37680000000000C_nR_1R_aR_b + 18877680000000000C_nR_2R_aR_b \\
0 \;=\; & \frac{300001884R_a + 300001884R_b}{5} + 6000000R_1R_a \\
& -308000000R_2R_a + 376800000CR_2R_a + 6000037680000CR_1R_2R_a \\
& +376800000CR_3R_a + 6000037680000CR_1R_3R_a \\
& -\,279962320000CR_2R_3R_a + 6000000R_1R_b - 308000000R_2R_b \\
& +\,376800000CR_2R_a + 6000037680000CR_1R_2R_a \\
& +\,376800000CR_3R_a + \;6000037680000CR_1R_3R_b \\
& -\,242282320000CR_2R_aR_b + 37680000000000CC_nR_1R_2R_aR_b \\
& +37680000000000CC_nR_1R_3R_aR_b + 18877680000000000CC_nR_2R_3R_aR_b \\
0 \;=\; & \frac{300001884CR_2R_a + 300001884CR_3R_a}{5} + 6000000CR_1R_2R_a + 60R_a \\
& +\frac{300001884CR_2R_b + 300001884CR_3R_b + 300001884C_nR_aR_b}{5} \\
& -6280R_2R_a + 6000000CR_1R_3R_a - 308000000CR_2R_3R_a + 60R_b \\
& -6280R_2R_b + 6000000CR_1R_2R_a + 6000000CR_1R_3R_b \\
& -308000000CR_2R_3R_b + 6000000C_nR_1R_aR_b - 308000000C_nR_2R_aR_b \\
& +376800000CR_2R_a + 6000037680000CR_1R_2R_a \\
& +376800000CC_nR_2R_aR_b + \;6000037680000CC_nR_1R_2R_aR_b \\
& +376800000CC_nR_3R_aR_b + \;6000037680000CC_nR_1R_3R_aR_b \\
& -242282320000CC_nR_2R_3R_aR_b \\
0 \;=\; & 60CR_2R_a + 60CR_3R_a - 6280CR_2R_3R_a + 60CR_2R_b + \;60CR_3R_b \\
& -6280CR_2R_3R_b + 60C_nR_aR_b - 6280C_nR_2R_aR_b \\
& +\frac{300001884CC_nR_2R_aR_b + 300001884CC_nR_3R_aR_b}{5} \\
& +6000000CC_nR_1R_3R_aR_b - 308000000CC_nR_2R_3R_aR_b \\
0 \;=\; & 60CC_nR_2R_aR_b + 60CC_nR_3R_aR_b - 6280CC_nR_2\;R_3R_aR_b
\end{aligned}
\tag{3.13}
$$

If we use NSolve command as a numerical engine, we obtain inappropriate solutions for the nonlinear equations in Eq. (3.13). Indeed the two numerical solutions were {R_1=0, R_2=0, R_3=0, C=0, R_a=2.41411e9, R_b=2.40405e9, C_n=0} or {R_1=0, R_2=11.152, R_3=0, C=0, R_a=4.29255e7, R_b=4.27468e7, C_n=0}. These circuit parameters are not adequate for design task.

Instead of computing directly estimations, we apply the Solve command to calculate symbolic solutions. We found four exact solutions and two parametric symbolic solutions in terms of R_a, voicing the explicit caveat: “Equations may not give solutions for all “solve” variables”. We obtained four reasonable and exact solutions. One of the solutions is shown in (3.14) and we omit the other solutions.

$$R_1 = \frac{94350069732743 + 3\sqrt{92119100053882035457181156 1}}{384801505000000}$$

$$R_2 = \frac{3\left(94350069732743 + 3\sqrt{92119100053882035457181156 1}\right)}{49875592162604}$$

$$R_3 = \frac{3\left(94350069732743 + 3\sqrt{92119100053882035457181156 1}\right)}{314(94191230267257) + 3\sqrt{9211910005388203545718156 1}}$$

$$R_b = \frac{917194231517257}{921029518482743} R_a$$

$$C_n = 0$$

$$C = \frac{3753664980267257 + 3\sqrt{92119100053882035457181156 1}}{36764475000000000000}$$

(3.14)

Then we numerically calculate the exact solution:

Solution 1 {R_1=0.481816, R_2=11.152, R_3=0.00956233, C=0.000104577, C_n=0, R_b=0.995836R_a }
The other solutions are:
Solution 2 {R_1=0.00856723, R_2=0.198294, R_3=0.0100378, C=0.0000996237, C_n=0, R_b=0.995836R_a }
Solution 3 {R_1=0.00793284, R_2=0.198034, R_3=0.0100384, C=0.000099617, C_n=2.00417e-6／R_a, R_b=0.995848R_a }
Solution 4 {R_1=0.48245, R_2=12.0438, R_3=0.00956233, C=0.000104584, C_n=2.00417e-6／R_a, R_b=0.995848R_a }.

We consider the meanings of these solutions. The symbolic values R_b, C_n as functions of R_a are circuit elements used to construct the feedback circuit described in Fig. 3.4. And C_n=0 of solution 1 and solution 2 indicates that the coefficient of the second term of the numerator and the fourth term of the denominator in polynomial T_{sys} are zero. That is a loss of generality from the perspective of the circuit. However, we substitute a value into R_a to obtain suitable parameters. For example, assuming that R_a=20000, then R_b=199167.2 from solution 2.

Another approach to obtaining a solution for the equation $T_{sys} = F_{sys}$ is to multiply as+b to equalize the degree of the numerator and denominator of F_{sys} and T_{sys}. Namely,

$$F_{sys}' = \frac{6000000(s+1000000)(as+b)}{(s^2+50000s^2+1000000000s+3000000000000)(as+b)} \quad (3.15)$$

Then we solve the following equation, $T_{sys} = F'_{sys}$. Here the numerator of T_{sys} is equal to the numerator of F'_{sys}, and the denominator of T_{sys} is equal to the denominator of F'_{sys}. As a result, we can obtain solution 3, R_a=2.4172688377894015e9. In brief, we obtained solution 4 without the loss of generality.

3.5 Conclusions

We discussed a method of analog circuit design using symbolic analysis. We derived a transfer function of the circuit characteristics for a power supply stabilization loop circuit which is a major component in power supply integrated circuit. We specified a circuit design target in the form of a transfer function. We then formulated as a problem to solve a system of nonlinear equations in order to decide the most suitable set of constants of circuit elements that satisfy this target by using symbolic computation package Mathematica [6]. As result of our investigation, we reveal that these equations could not be solved with numerical methods but they could be solved with the symbolic algebraic methods and that there are plural solutions which have important meaning from a circuit design perspective point of view.

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Chapter 4
Equation-Based Technique of Electro-thermal Modeling and Reliability Circuit Analysis of Power MOSFETs

4.1 Introduction

Recently, we proposed a technique for simple electro-thermal equivalent circuit level modeling and reliability circuit simulation of power MOSFETs (MOSFETs) with SystemC-AMS/NGSPICE [13] [18]. As a case study, we focused on an Unclamped Inductive Switching (UIS) test circuit that is used for an avalanche breakdown test of MOSFETs. The avalanche breakdown (breakdown) is affected by device junction temperature rise that is due to self-heating of MOSFETs. In the reliability circuit simulation, it is essential that coupling of the electrical behaviour and thermal behaviour (electrical-thermal coupling) is considered [5] [9] [10] [15] [16] [19].

The goal of our research in this section is to present a new technique equation-based electro-thermal coupling modeling and transient (time domain) analysis of MOSFETs with Mathematica [11]. First we derive a system of ordinary differential equations, which express the current-voltage characteristics (I-V characteristics) and the electrical-thermal coupling of MOSFETs. Next we implement the system into Mathematica, and solve it. Finally we demonstrate our technique by several test results with the UIS test circuit.

In the next section 4.2, we explain an Unclamped Inductive Switching (UIS) test circuit. Section 4.3 describes our equation-based electro-thermal power MOSFET model and circuit analysis technique with Mathematica. Section 4.4 describes our experiments and compares the results. We conclude our research in Section 4.5.

NOMENCLATURE

Power MOSFET

t	Simulation time domain [sec]
T_{nom}	Room temperature [K]
β	MOSFET channel conductance [A/V^2]
β_0	Value of β at T_{nom} [A/V^2]
V_{th}	Threshold voltage [V]
V_{th0}	Value of V_{th} at T_{nom} [V]
V_{gs}	Gate-source voltage [V]
V_{ds}	Drain-source voltage [V]
C_{gs}	Gate-source capacitance [F]
C_{ds}	Drain-source capacitance [F]
C_{gd}	Gate-drain capacitance [F]
$R_{on(mos)}$	Drain-source on resistance [Ohm]
$R_{off(mos)}$	Drain-source off resistance [Ohm]
R_{ds}	Drain-source resistance [Ohm]
G_{ds}	Drain-source conductance [1/Ohm] ($R_{ds} = 1/G_{ds}$)
I_{ds}	Drain-source current [A]
TCV_{th}	Temperature coefficient of V_{th} [1/K]

$TC\beta$ Temperature coefficient of β [-]
BV_{dss} Avalanche breakdown voltage at T_{nom} [V]
$BV_{dss(eff)}$ Effective avalanche breakdown voltage [V]
R_{mos_body} MOSFET body resistance [Ohm]
V_{dd} Power supply voltage [V]
V_{gg} Pulse voltage source [V]
L_{drain} Drain load inductance [H]
R_{drain} Drain load resistance [Ohm]
R_{gate} Gate resistance [Ohm]
P_{mos} MOSFET power dissipation [W]
T_j Device junction temperature [K]
(Nodal voltage at thermal node)

Diode
V_{on} Diode on voltage [V]
V_{pn} Diode pn junction voltage [V]
$R_{on(diode)}$ Diode on resistance [Ohm]
$R_{off(diode)}$ Diode off resistance [Ohm]
$R_{on(body)}$ Body diode on resistance [Ohm]
$R_{off(body)}$ Body diode off resistance [Ohm]
$R_{on(bkdn)}$ Breakdown diode on resistance [Ohm]
$R_{off(bkdn)}$ Breakdown diode off resistance [Ohm]
V_{br} Breakdown voltage [V] ($V_{br}= BV_{dss(eff)}$)

Thermal Circuit
T_{thi} Device junction-case temperature rise [K]
C_{thi} Device junction-case thermal capacitance [J/K]
R_{thi} Device junction-case thermal resistance [K/W] (The index i ranges as $i = 1, 2, \ldots, 6$)
T_{case} Case temperature [K]
T_{amb} Ambient temperature [K] ($T_{amb}= T_{nom}$)
V_{amb} Ambient temperature definition [K] ($V_{amb} = T_{amb}$)
T_{thp} Case-ambient temperature rise [K] ($T_{thp} = T_{case} - T_{nom}$)
C_{thp} Case-ambient thermal capacitance [J/K]
R_{thp} Case-ambient thermal resistance [K/W]

4.2 Unclamped Inductive Switching Test Circuit

An UIS test circuit is used to evaluate tolerance for the avalanche breakdown (breakdown) that is the most important reliability assessment of power MOSFETs. Figure 4.1 depicts the schematic of the UIS test circuit that is used in [5] [9] [10] [13]. The UIS test circuit is a steep switching circuit that is composed of a MOSFET (switching device), and a parasitic inductor (load device). The counter electromagnetic force that is induced by the inductance causes a significant over voltage transient between drain and source of the MOSFET. If the resulting voltage transient is large enough, the MOSFET is forced into the drain-source avalanche breakdown. The high drain-source current causes its device junction temperature rise that is due to self-heating effect. The device junction temperature rise affects the avalanche breakdown voltage and electrical characteristics of the MOSFET [9] [10] [13] [15].

It is very important that the device junction temperature rise that is due to self-heating effect is reflected to the MOSFET characteristics. In the UIS test circuit, particularly, the on/off

switching drain-source resistance and avalanche breakdown of the MOSFET are important characteristics, which have temperature dependence. Therefore, the electro-thermal device model that incorporates with the self-heating effect and electrical characteristics is essential in the UIS test circuit simulation for tolerance evaluation of the avalanche breakdown [5] [9] [10] [13].

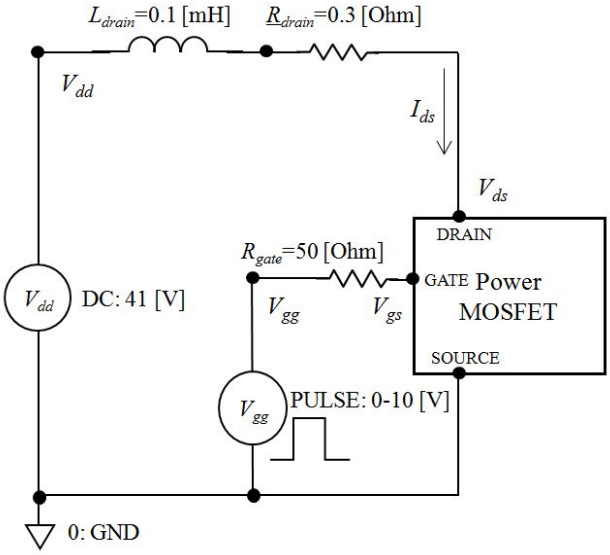


Figure 4.1: Unclamped Inductive Switching test circuit [5] [9] [10] [13].

4.3 Our Equation-Based Modeling

We apply our equation-based modeling to an UIS circuit. The circuit is composed of an electronic circuit and a thermal circuit, as depicted in Fig. 4.2. The electronic circuit include a power MOSFET and its simple electrical equivalent circuit model is depicted in Fig. 4.3 [13]. And the thermal circuit include a thermal equivalent circuit model from device junction (T_j) to package case (T_{case}), which is depicted in Fig. 4.3.

The power dissipation (G_{mos_pwr}) of the MOSFET flows into the thermal equivalent circuit model as a current source, and the device junction temperature (T_j) is calculated as a nodal voltage. The device junction temperature is fed back to the electrical equivalent circuit model as thermal nodal voltage of the MOSFET. Then, the values of very important parameters with (device) temperature dependence such as threshold voltage, channel conductance (G_{ds}), effective avalanche breakdown voltage ($BV_{dss(eff)}$), and so on are updated.

Based on the updated values, next computation process goes. A series of computation processes is repeated at each time step in electro-thermal circuit analysis. The thermal equivalent circuit model is a linear network that composed of thermal resistances (R_{thi}) and thermal capacitances (C_{thi}), which expresses thermal conduction from device junction (T_j) to package case (T_{case}). Note that i = 1, 2, …, 6. And the thermal conduction from package case (T_{case}) to ambient (T_{amb}) is expressed as a linear circuit that compose of a thermal resistance (R_{thp}) and a thermal capacitance (C_{thp}).

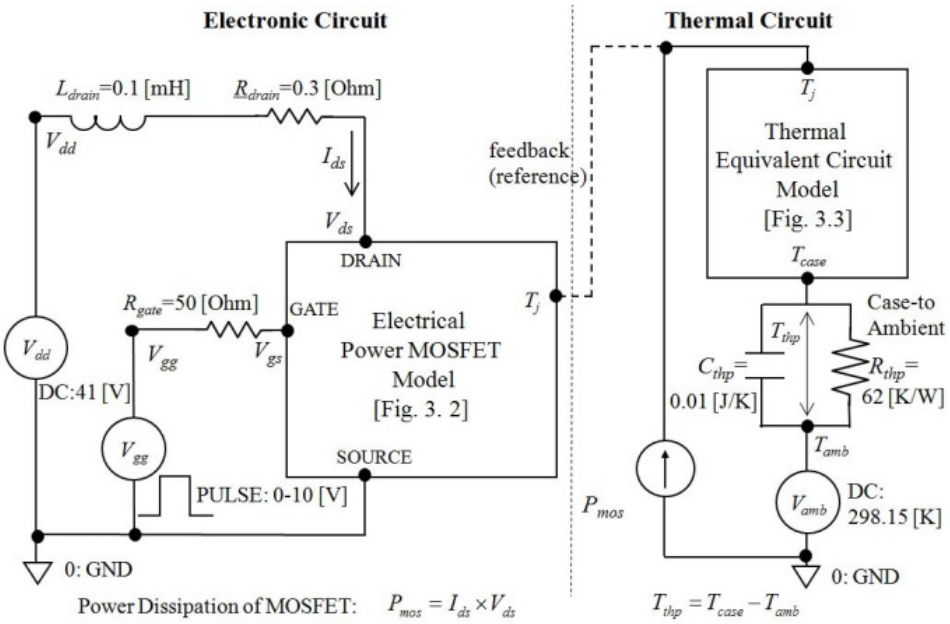


Figure 4.2: Schematic for the electro-thermal simulations of an UIS test circuit.

We model the UIS test circuit depicted in Fig. 4.2 as a system of ordinary differential equations.

Note that source node (SOURCE) is connected to ground (GND). First we define a drain-source function that expresses the drain-source conductance of the MOSFET (G_{ds}), and express it as Eq. (4-1). The function is equivalent to the current-voltage (I-V) characteristics of the MOSFET, and is used at our simple power MOSFET electrical model [13] depicted in Fig. 3.2. It has temperature dependence such as threshold voltage and channel conductance, which is described by Eqs. (4-2) and (4-3).

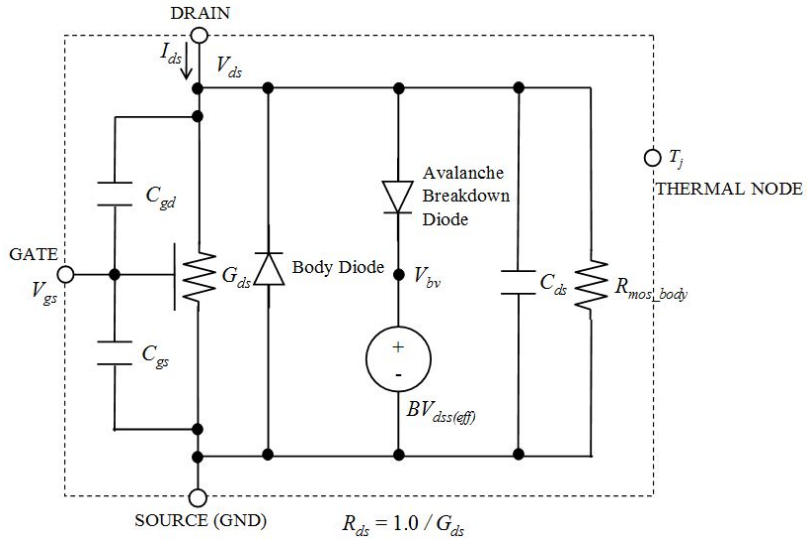


Figure 4.3: Our simple electrical power MOSFET model [13].

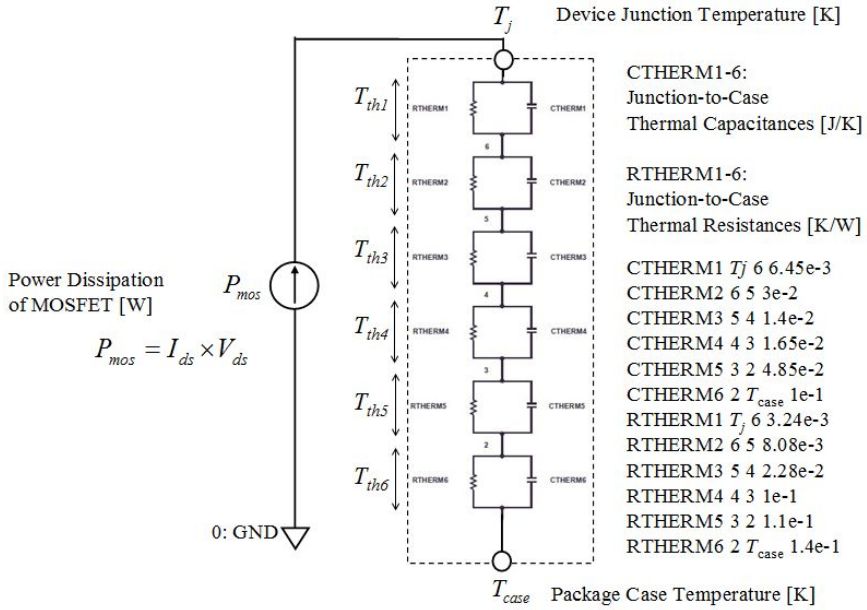


Fig. 4.4: Thermal equivalent circuit model of electro-thermal power MOSFET model [5] [9] [10].

$$G_{ds}(V_{gs}, V_{th}, \beta, R_{off(mos)}) := Max(Tanh(V_{gs} - V_{th}), 0.0) \times \beta(V_{gs} - V_{th}) + \left(\frac{1.0}{R_{off(mos)}}\right) \tag{4-1}$$

where

$$V_{th} = V_{th0} \times (1.0 + TCV_{th} \times (T_j - T_{nom})) \tag{4-2}$$

$$\beta = \beta_0 \times \left(\frac{T_j}{T_{nom}}\right)^{TC\beta} \tag{4-3}$$

Note that the drain-source resistance (R_{ds}) of the MOSFET is the inverse number of drain-source conductance (G_{ds}).

Next we define a diode function that expresses the voltage-current (V-I) characteristics of the diode device, and express it as Eq. (4-4). It is used to describe the characteristics of two diodes (body diode and breakdown diode) that are depicted in Fig. 4.3.

$$i_{diode}(V_{pn}, V_{on}, R_{on(diode)}, R_{off(diode)}) := \left[Max(Tanh(V_{pn} - V_{on}), 0.0) \times \left(\frac{1.0}{R_{on(diode)}}\right) + \left(\frac{1.0}{R_{off(diode)}}\right)\right] \times V_{pn} \tag{4-4}$$

In the following, we derive a system of ordinary differential equations to express the electrical characteristics and self-heating effect of the MOSFET.

As depicted in Fig. 4.2, the drain-source current (I_{ds}) flows along a drain inductance (L_{drain}) and a drain resistance (R_{drain}), and it is described by an ordinary differential equation of Eq. (4-5).

$$V_{dd} - V_{ds} = L_{drain} \frac{dI_{ds}}{dt} + R_{drain} \times I_{ds} \tag{4-5}$$

As depicted in Fig. 4.2 and Fig. 4.3, the KCL (Kirchhoff's Current Law) with respect to gate node (V_{gs}) is expressed as Eq. (4-6).

$$\frac{V_{gg}-V_{gs}}{R_{gate}}=\left(C_{gd}+C_{gs}\right)\frac{dV_{gs}}{dt}-C_{gd}\frac{dV_{ds}}{dt} \tag{4-6}$$

As depicted in Fig. 4.3, the KCL with respect to drain node (V_{ds}) is expressed as Eq. (4-7). Note that it uses the functions defined by Eq. (4-3) and Eq. (4-4).

$$\begin{aligned}&-C_{gd}\frac{dV_{gs}}{dt}+\left(C_{gd}+C_{ds}\right)\frac{dV_{ds}}{dt}+G_{ds}\left(V_{gs},V_{th},\beta,R_{off\,(mos)}\right)\times V_{ds}\\&-i_{diode}\left(-V_{ds},V_{on(body)},R_{on(body)},R_{off\,(body)}\right)\\&+i_{diode}\left(V_{ds}-V_{bv},V_{on(bkdn)},R_{on(bkdn)},R_{off\,(bkdn)}\right)+\frac{V_{ds}}{R_{body}}=I_{ds}\end{aligned} \tag{4-7}$$

The temperature dependence of effective avalanche breakdown voltage ($BV_{ds(eff)}$) is used at our simple electrical power MOSFET model depicted in Fig. 4.3, and it is expressed as Eq. (4-8) [13].

$$BV_{ds(eff)}=BV_{ds}\times\left(1.0+9.5e-4\times\left(T_j-T_{nom}\right)+1.0e-7\times\left(T_j-T_{nom}\right)^2\right) \tag{4-8}$$

As depicted in Fig. 4.2 and Fig. 4.4, the power dissipation ($G_{\mathrm{mos\_pwr}}$) of the MOSFET flows into the thermal equivalent circuit model, which is a simple linear network that composed of thermal resistances and thermal capacitances. Therefore, it is expressed as Eq. (4-9). Furthermore, by using the device junction-case temperature rise (T_{thi}), the case-ambient temperature (T_{thp}), and ambient temperature (T_{amb}), the device junction temperature (T_j) is calculated by Eq. (4-10).

$$\left.\begin{aligned}&P_{mos}=I_{ds}\times V_{ds}\\&C_{th1}\frac{dT_{th1}}{dt}+\frac{T_{th1}}{R_{th1}}=P_{mos}\\&C_{th2}\frac{dT_{th2}}{dt}+\frac{T_{th2}}{R_{th2}}=P_{mos}\\&C_{th3}\frac{dT_{th3}}{dt}+\frac{T_{th3}}{R_{th3}}=P_{mos}\\&C_{th4}\frac{dT_{th4}}{dt}+\frac{T_{th4}}{R_{th4}}=P_{mos}\\&C_{th5}\frac{dT_{th5}}{dt}+\frac{T_{th5}}{R_{th5}}=P_{mos}\\&C_{th6}\frac{dT_{th6}}{dt}+\frac{T_{th6}}{R_{th6}}=P_{mos}\\&C_{thp}\frac{dT_{thp}}{dt}+\frac{T_{thp}}{R_{thp}}=P_{mos}\end{aligned}\right\} \tag{4-9}$$

$$T_j=T_{th1}+T_{th2}+T_{th3}+T_{th4}+T_{th5}+T_{th6}+T_{thp}+T_{amb} \tag{4-10}$$

In Section 4.4, we verify our equation-based modeling and electro-thermal coupling circuit

analysis with respect to the UIS test circuit.

4.4 Experimental Results

As described above, we derived the system of ordinary differential equations. We develop a notebook source code and implement it into Mathematica. (See the source code of Fig.4.6.) We define two node voltages (V_{gs}, V_{ds}), drain-source current (I_{ds}), six device junction-case temperature rises ($T_{th1,}$ $T_{th2,}$ $T_{th3,}$ $T_{th4,}$ $T_{th5,}$ T_{th6}), and case-ambient temperature rise (T_{thp}) as unsolved variables. The initial values at time domain t=0 of these unsolved variables are set in the following: V_{gs}=0.0 [V], V_{ds}=0.0 [V], I_{ds}=0.0 [A], T_{th1}=0.0 [K], T_{th2}=0.0 [K], T_{th3}=0.0 [K], T_{th4}=0.0 [K], T_{th5}=0.0 [k], T_{th6}=0.0 [K].

Furthermore, the value of each parameter in the system of ordinary differential equations is set the same as that of our previous work presented with [13]. Note that the parameter values are based on the datasheet and application notes [5] [9] [10] released by Fairchild Semiconductor. (See [13] for more details.) We show the values of main model parameters and temperature coefficients at room temperature in the following: L_{drain}=0.1e-3 [H], R_{drain}＝0.3 [Ohm], V_{dd}=41.0 [V], C_{ds}=2.65e-9 [F], C_{gs}=4.40e-9 [F], C_{gd}=1.70e-9 [F], R_{gate}=50.0 [Ohm], T_{nom}=298.15 [K], V_{th0}=2.8 [V], $R_{off(mos)}$=1.0e12 [Ohm], R_{mos_body}=1.0e15 [Ohm], V_{th0}=2.8 [V], β_0=40.0 [A/V2], BV_{dss}=69.3 [V], TCV_{th}=-3.57 [1/K], and $TC\beta$=-2.1 [-], $R_{on(body)}$=0.118 [Ohm], $R_{off(body)}$ =1.0e12 [Ohm], $R_{on(bkdn)}$=0.118 [Ohm], $R_{off(bkdny)}$ =1.0e12 [Ohm], V_{on}=0.6 [V], V_{br}=BV_{dss}, C_{th1}=6.45e-3 [J/K], C_{th2}=3.00e-2 [J/K], C_{th3}=1.40e-2 [J/K], C_{th4}=1.65e-2 [J/K], C_{th5}=4.85e-2 [J/K], C_{th6}=1.00e-1 [J/K], C_{thp}=1.00e-2 [J/K], R_{th1}=3.24e-3 [K/W], R_{th2}=8.08e-3 [K/W], R_{th3}=2.28e-2 [K/W], R_{th4}=1.00e-1 [K/W], R_{th5}=1.10e-1 [K/W], R_{th6}=1.40e-1 [K/W], R_{thp}=62.0 [K/W], T_{amb}= T_{nom}.

As our experimental verification, we ran the circuit analysis with Mathematica on HP dv9700 (OS Windows 7, CPU Intel(R) Core(TM) 2.5GHz, RAM 8.00 GB). And we obtained the solutions for the unsolved variables by numerical module NDsolve( ), and its run time (CPU time) is 91.2 [sec]. Fig. 4.5 (1) depict the circuit analysis results in the time domain. The value of the device junction temperature (T_j) is calculated with the values of size device junction-case temperature rises ($T_{th1,}$ $T_{th2,}$ $T_{th3,}$ $T_{th4,}$ $T_{th5,}$ T_{th6}) and case-ambient temperature rises ($T_{thp,}$ T_{amb}) by Eq. (3-10). Note that the device junction temperature (T_j) is expressed by unit of deg. C in the Fig. 4.5.

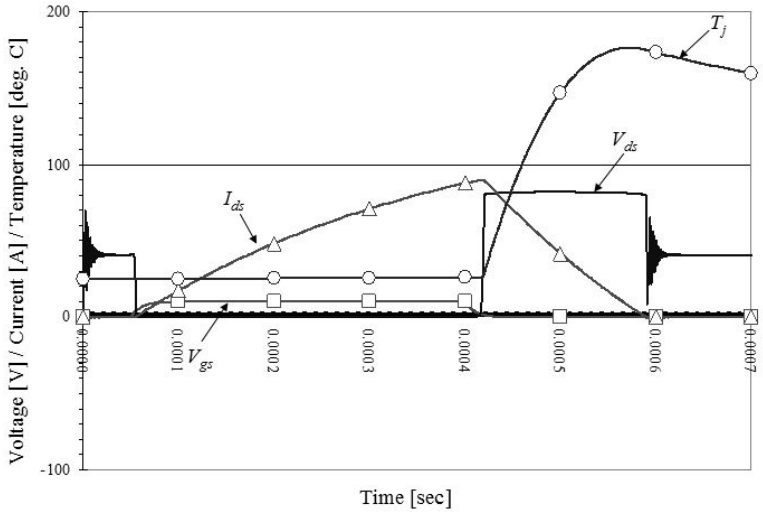
As other reference, we used an accurate PSPICE electro-thermal power MOSFET model [5], [9]-[10] released by Fairchild Semiconductor, and simulated the same UIS test circuit depicted in Fig. 4.2, with a powerful circuit simulator called TINA-TI (Texas Instruments version of PSPICE) [17] from Texas Instruments. In this case, the run time with the same computer mentioned above is 26.5 [sec]. Fig. 4.5 (2) depict the circuit simulation results obtained by TINA-TI.

Furthermore, we used a very simple XSPICE electro-thermal power MOSFET model [13] released by our previous work, and simulated the same UIS test circuit depicted in Fig. 4.2, with a free circuit simulator called NGSPICE/XSPICE from the gEDA Project [14] and the Georgia Institute of Technology. [20]. In this case, the run time with the same computer mentioned above is 6.1 [sec]. Fig. 4.5 (3) depict the circuit simulation results obtained by NGSPICE/XSPICE.

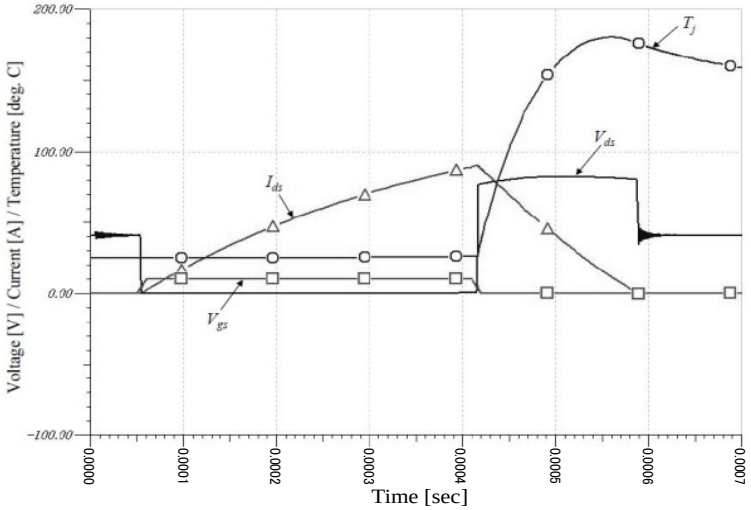
As depicted in Fig. 4.5 (1), the circuit analysis results on our equation-based modeling with Mathematica have some oscillations. But they are almost consistent with those of other two reference cases, and hence demonstrate the adequacy of our technique for electro-thermal modeling and circuit analysis.

However, its run time increases more than those of other two cases. The reason is due to the

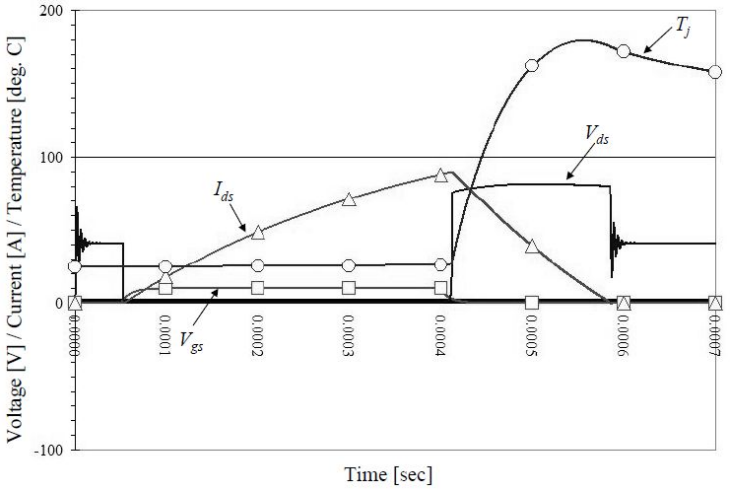
performance of the numerical solver (NDsolve( )) of Mathematica.



(1) Mathematica with our equation-based model



(2) TINA-TI (PSPICE) with accurate model of [5] [9] [10]



(3) NGSPICE/XSPICE with our simple model of [13]

Figure4.5: Simulation results of UIS test circuit.

4.5 Conclusions

We have proposed a new technique for the electro-thermal modeling and reliability circuit analysis with Mathematica. It starts with the modeling of a power MOSFET circuit as a system of ordinary differential equations, and uses a numerical solver of Mathemtica to obtain a solution of the system.

Furthermore, we applied our technique to electro-thermal and reliability circuit analysis of an UIS test circuit. Our technique was demonstrated by experimental results. They also revealed that the numerical solver of Mathematica is capable of circuit analysis such as that of SPICE (a circuit simulator)..

However the solver is more than 10 times slower than that of SPICE. We are improving the solver of Mahematica in order to reduce the run time.

```
(*** diode function ***)
id[Vpn_,Von_,Rondiode_,Roffdiode_]=(Max[Tanh[Vpn-Von],0.0]*(1.0/Rondiode)+(1.0/Roffdiode))*Vpn;
(*** mos drain-source conductance function ***)
Gds[Vgs_,Vth_,β_,Roffmos_,Tjuncnom_,Tjunc_,TCB_,TCV_]=(Max[Tanh[Vgs-Vth*(1.0+TCV*(Tjunc-Tjuncnom))],0.0]*β*(Tjunc/Tju
ncnom)^TCB*(Vgs-Vth*(1.0+TCV*(Tjunc-Tjuncnom)))+(1.0/Roffmos));
(*** gate input pulse function ***)
fpulse[x_Real,delay_,rise_,width_,fall_,periode_,lowval_,highval_]=Which[x<=delay,lowval,
Mod[x-delay,periode]>rise+width+fall,lowval,
Mod[x-delay,periode]>rise+width,(lowval-highval)/fall*(Mod[x-delay,periode]-rise-width)+highval,
Mod[x-delay,periode]>rise,highval,
Mod[x-delay,periode]>0.0,(highval-lowval)/rise*(Mod[x-delay,periode])+lowval,
Mod[x-delay,periode]<=0.0,lowval];
(*** device junction temperature ***)
Tj[DTp_,DT6_,DT5_,DT4_,DT3_,DT2_,DT1_]=DTp+DT6+DT5+DT4+DT3+DT2+DT1+298.15;
(*** unsolved variables ***)
Clear[i, vg, vd,Tp,T6,T5,T4,T3,T2,T1];
(*** a system of ordinary differential equations for an electronic circuit ***)
eqns={Ldrain*(i^')[t]==Vdd-vd[t]-Rdrain*i[t],
(Cgd+Cgs)*vg'[t]-Cgd*vd'[t]==(fpulse[t,Delay,Rise,Width,Fall,Periode,Lowval,Highval]-vg[t])/Rgate,
-Cgd*vg'[t]+(Cgd+Cds)*vd'[t]==0.0-Gds[vg[t],Vth,β,Roffmos,Tnom,Tj[Tp[t],T6[t],T5[t],T4[t],T3[t],T2[t],T1[t]],TCB,TCV]*vd[t]+id[0.0
-vd[t],Von,Rondiode,Roffdiode]-id[vd[t]-(Vbv*(1.0+9.5*10^-4*(Tj[Tp[t],T6[t],T5[t],T4[t],T3[t],T2[t],T1[t]]-Tnom)+1.0*10^-7*(Tj[Tp
[t],T6[t],T5[t],T4[t],T3[t],T2[t],T1[t]]-Tnom)^2)),Von,Rondiode,Roffdiode]-vd[t]/Rbody+i[t],
(*** a system of ordinary differential equations for a thermal circuit ***)
Cthp*Tp'[t]==i[t]*vd[t]-Tp[t]/Rthp,
Cth6*T6'[t]==i[t]*vd[t]-T6[t]/Rth6,
Cth5*T5'[t]==i[t]*vd[t]-T5[t]/Rth5,
Cth4*T4'[t]==i[t]*vd[t]-T4[t]/Rth4,
Cth3*T3'[t]==i[t]*vd[t]-T3[t]/Rth3,
Cth2*T2'[t]==i[t]*vd[t]-T2[t]/Rth2,
Cth1*T1'[t]==i[t]*vd[t]-T1[t]/Rth1,
(*** initialization ***)
i[0]==0.0, vd[0]==0.0, vg[0]==0.0, Tp[0]==0.0, T6[0]==0.0, T5[0]==0.0, T4[0]==0.0, T3[0]==0.0, T2[0]==0.0, T1[0]==0.0
};
(*** input parameters ***)
eqns =
eqns/.{Ldrain->1.0*10^-4,Rdrain->0.3,Vdd->41.0,Cgd->1.7*10^-9,Cgs->4.4*10^-9,Cds->2.65*10^-9,Rgate->50.0,Delay->0.05*10
^-3,Rise->0.01*10^-3,Width->0.35*10^-3,Fall->0.01*10^-3,Periode->1.0*10^-3,Tnom->298.15,
Lowval->0.0,Highval->10.0,Vth->2.8,β->40.0,Roffmos->1.0*10^12,Von->0.6,Vbv->69.3,Rondiode->0.118,Roffdiode->1.0*10^12,
Rbody->1.0*10^15,Cthp->1.0*10^-2,Rthp->62.0,Cth6->1.0*10^-1,Rth6->1.4*10^-1,Cth5->4.85*10^-2,Rth5->1.1*10^-1,Cth4->1
.65*10^-2,Rth4->1.0*10^-1,Cth3->1.40*10^-2,Rth3->2.28*10^-2,Cth2->3.00*10^-2,Rth2->8.08*10^-3,Cth1->645*10^-3,Rth1->
3.24*10^-3,TCB->-2.1,TCV->-3.57*10^-3} ;
(*** call NDSolve() ***)
sol[v_]:= NDSolve[(eqns)/. Vdd->v,{i,vg, vd,Tp,T6,T5,T4,T3,T2,T1},{t,0,2.0*10^-3},MaxStepSize->0.1,MaxSteps->1000000];
```

```
(*** plots ***)
Do[Print[Plot[Evaluate[vd[t]/. sol[Vdd]],{t,0,2.0*10^-3},PlotLabel->Vdd]],{Vdd,41.0,41.0,41.0}];
Do[Print[Plot[Evaluate[i[t]/. sol[Vdd]],{t,0,2.0*10^-3},PlotLabel->Vdd]],{Vdd,41.0,41.0,41.0}];
Do[Print[Plot[Evaluate[Tj[Tp[t],T6[t],T5[t],T4[t],T3[t],T2[t],T1[t]]-273.15/.
sol[Vdd]],{t,0,2.0*10^-3},PlotLabel->Vdd]],{Vdd,41.0,41.0,41.0}];
```

Figure 4.6: Our notebook source codes with Mathematica.

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Chapter 5
Equation-Based Circuit Design Technique for DC/DC Converters with Symbolic Computation System

5.1 Introduction

DC/DC converters are very important electronic circuits for power management ICs. They convert one input direct current (DC) voltage level, and generate another output DC voltage level. And they have been widely used in portable electronic devices such as smart phones and personal computers that are supplied with power from batteries. Today, DC/DC converters are essential parts of ECU (Engine Control Unit) for automotive application [9]-[10] [24]-[26]. In this chapter, we present a new technique of equation-based circuit design for DC/DC converters.

We briefly review previous main research activities with respect to equation-based circuit design. In the area of analog electronic circuits, so far several methods of equation-based circuit design have been proposed for efficiency of the circuit design. In particular a method using GP (Geometric Programming) has attracted considerable attention [19]-[21] [31]-[32]. The method simplifies the circuit equations and device model equations into first-order or second-order approximations, and formulates a circuit design problem as a constrained optimization problem. It applies a global optimization algorithm by GP in order to solve the problem, and obtains optimized design parameters (equations parameters) for the circuit design specification. This method using GP has been applied in CMOS circuit designs such as op-amps (operational amplifiers) [19]-[21] [31]-[32], pipelined ADC [37], and DC/DC buck converter [36]. However the method has the disadvantages of being not able to deal with non-convex problems that are important in many design cases, and causes errors between optimized results and circuit simulation results in deep-submicron devices region [18].

On the other hand, an equation-based method with symbolic analysis has been proposed. The scope of this method is restricted to the analysis of linear or weak nonlinear circuits in such frequency domain as the Laplace domain (s-domain) and the z-domain. It extracts a mathematical representation for the circuit in terms of the transfer functions by using symbolic computation (symbolic manipulation). The transfer functions extracted are implemented into computer algebra system, such as Mathematica, and the frequency and phase responses of the circuit are computed [22]-[23].

In the research of [23], the concepts and techniques of symbolic analysis for analog circuits are introduced, and are implemented as a symbolic simulator program called ISAAC (Interactive Symbolic Analysis of Analog Circuits), which have been developed by Katholieke University Leuven. ISAAC is able to analyze lumped, linear, time-invariant circuits in the complex frequency domain, and return the circuit symbolic transfer functions and the circuit elements represented by symbols. In the research of [22], the capabilities of computer algebra systems (CAS) are illustrated by application examples in analog circuit design, such as a low pass filter, a BJT amplifier, and an LC ladder.

Furthermore, in the research of [16], the basic principle of symbolic circuit analysis is presented. And it is discussed the implementation technique using a computer algebra tool Mathematica. In the research of [42], new software for symbolic analysis and symbolic designs of signal processing system (digital filter) is presented, and is implemented into Mathematica. Recently some tools for analog circuit design and simulation using symbolic circuit analysis

have been developed [13]-[15]. In the research of [38], as a new attempt, it has been proposed a new symbolic verification methodology for analog and mixed signal (AMS) design, and has been applied in a third order Delta-Sigma (DS) modulator.

However in the equation-based method with symbolic analysis described above, in most cases, the targets of analysis are limited to relatively simple linear analog circuits such as RLC ladder, op-amps, analog filter, and digital filter (z-domain) [13]-[16] [22]-[23] [38] [42]. It does not deal with practical industrial analog circuit design. And, the differences of results between symbolic circuit analysis and numerical circuit simulation also have been not adequately verified.

In the area of DC/DC converters, a few symbolic analysis program packages have been developed. They generate the averaged model automatically, from a netlist composed of a converter topology and some inputs describing the operation of the converter, and simulate it [17] [39]-[41]. However the disadvantage of this model is that it does not consider the feedback control loop for phase compensation used in DC/DC converters.

So far, in our research of [12], we have developed a simplified circuit model equation for describing the characteristics of a DC/DC converter including a (switching) feedback control loop. And we have presented a technique optimizing circuit model parameters in order to satisfy a design specification by using a computer algebra program Mathematica [29]. The feedback control loop is a most essential part in DC/DC converters. The adjustment of the frequency response of this feedback control loop, which is called loop compensation, is needed to assure loop stability and optimize the transient response of the power supply. The frequency response is determined by the gain, phase, and crossover frequency of the loop reaction to the changes in load current at all frequencies. A Bode Plot is used to show the gain and phase of the frequency response [12] [17] [44].

The loop compensation is very sensitive to the characteristics of the output capacitor in the feedback control loop. The gain of the loop is largely dependent upon an effective capacitance in the output capacitor. And the phase margin is largely dependent upon a stray resistance, which is called ESR (equivalent series resistance), in the output capacitor.

Therefore, in the circuit design of DC/DC converters, an optimal output capacitor is needed in order to stabilize the loop [1]-[4] [5]-[8] [11] [33]-[35] [44]. Furthermore, the ESR influences also the ripple output voltage [43].

Under the above mentioned background, we propose an equation-based circuit design technique for DC/DC converters. In particular, it focuses on the optimization of the parameters in the output capacitor, which is composed of the ESR and the effective capacitance. The technique we present can be applied to a wide variety of DC/DC converter. But in this work, first we consider a buck converter that has a loop compensation system called as type III-B Compensator [1] [3] [4], as a typical case of Step-down DC/DC converter, and derive a detailed transfer function to model accurately the characteristics in the frequency domain (s-domain). Next we consider the relationship between the ESR and the effective capacitance with respect to MLCC (Multi Layer Ceramic Capacitor) capacitor [5] [33]-[35], which is a kind of output capacitors. And, we develop a new optimization procedure using a parameter sweep technique and apply it to the combination of the transfer function and the governing equation of ESR, and determine the optimal MLCC capacitor to satisfy the design specification of the buck DC/DC converter.

We implemented our technique described above into Scilab [30] as an equation-based design program for buck DC/DC converters. In our experiments, we applied the program to the circuit design of a practical industrial buck DC/DC converter, and obtained frequency responses by sweeping the parameter that is correspond to the ESR and the effective capacitance of MLCC capacitor. And we selected the optimal parameter to be satisfied the design specification.

Furthermore, as the comparison with existing circuit simulation method, under the same conditions and settings, we ran frequency-domain analysis in netlist-level on a power electronics circuit simulator, which is called as SIMPLIS [27]. The results of frequency responses by our program are in accord with those of the circuit simulator. This implies that our technique produces correct results. And our program is 70 times faster than SIMPLIS. These results demonstrate that our technique has the capacity of dealing with the practical industrial design/analysis, and its performance is comparable to that of the power electronics circuit simulator.

In the next section, we explain a buck DC/DC converter that has a loop compensation called as type III-B Compensator, and derive an accurate transfer function. Section 5.3 describes the characteristics of MLCC capacitor. Section 5.4 describes our technique for the optimization of MLCC capacitor, and implements it into Scilab. Section 5.5 describes our experiments and compares the results. We conclude our research in Section 5.6.

NOMENCLATURE

f	Frequency domain [Hz]
s	Complex number in the Laplace transform [-]
R_{ESR}	ESR (equivalent series resistance) of the output capacitor [V]
C_o	Effective capacitance of the output capacitor [F]
DF	Dissipation factor of the output capacitor [-]
α_{ESR}	Fitting parameter of the output capacitor [-]
V_{in}	Input voltage of the buck converter [V]
V_{out}	Output voltage of the buck converter [V]
I_o	Maximum output current [A]
V_{osc}	Peak to peak amplitude of the oscillator of the PWM (pulse width modulation) [V]
d	Duty ratio of the output pulse of the PWM [-]
V_e	Output voltage of the error-amplifier [V]
V_{ref}	Reference voltage the error-amplifier [V]
R_{Load}	Load resistance [Ohm]
F_s	Switching frequency [Hz]
F_0	Unity gain frequency (Zero cross frequency) [Hz]
F_{LC}	Double pole at the resonance frequency of the LC filter [Hz]
F_{ESR}	Zero produced by the ESR of the output capacitor [Hz]
$G_p(s)$	Transfer function of the power stage
$G(s)$	Transfer function of the power stage including the PWM
$W(s)$	Transfer function of the PWM generator
$H(s)$	Transfer function of the compensation network
$M(s)$	Transfer function of the whole loop gain of the buck converter
F_{z1}	First zero of the compensation network [Hz]
F_{z2}	Second zero of the compensation network [Hz]
F_{p1}	First pole of the compensation network [Hz]
F_{p2}	Second pole of the compensation network [Hz]
F_{p3}	Third pole of the compensation network [Hz]
C_{c1}	First capacitor of the compensator [F]
C_{c2}	Second capacitor of the compensator [F]
R_{c1}	First resistor of the compensator [Ohm]
R_{f1}	First feedback resistor of the compensator [Ohm]

R_{f2}	Second feedback resistor of the compensator [Ohm]
R_{f3}	Third feedback resistor of the compensator [Ohm]
C_{f3}	Feedback capacitor of the compensator [F]
Θ	Maximum phase lead of the compensator [degree]

5.2 Our Equation Based Modeling

5.2.1 Buck Converter

Buck converters are also called Step-down converters. They are used to step a input direct current (DC) voltage down from a higher level to a lower level. We consider a synchronous buck converter with voltage-mode control and voltage-mode error-amplifier as depicted in Fig. 5.1. The synchronous buck converter is composed of two power MOSFETs, an output inductor, an output capacitor, and a feedback control loop for phase compensation. This specific buck topology derives its name from the control method of the two power MOSFETs. The on-off control is synchronized in order to provide a regulated output voltage. And it prevents that the two power MOSFETs turn on at the same time. The feedback control loop is composed of an error-amplifier, a type III-B compensation network (type III-B Compensator [1]), and a PWM generator.

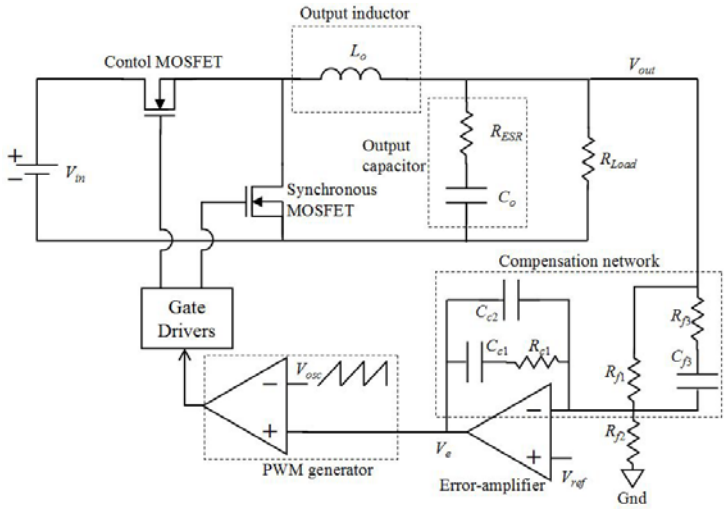


Figure 5.1: Circuit schematic of a synchronous buck converter with a voltage-mode error-amplifier.

5.2.2 Transfer Function

The circuit of the synchronous buck converter depicted in Fig. 5.1 is able to be modeled with large three blocks. Fig. 5.2 depicts the block diagram of the synchronous buck converter. The power stage (G_p (s)) comprises the two power MOSFETs, the drivers the output inductor, the output capacitor and the load resistance. The model of the PWM generator (W (s)) is expressed as the reciprocal of the peak to peak amplitude of the oscillator (V_{osc}) [1]. The compensator block (H (s)) is composed of the error-amplifier and the compensation network as depicted in Fig. 5.3. Furthermore, the power stage including the PWM (G (s)) is defined as a product of W

(s) and G_p (s).

In the following, we derive these transfer functions. Note that we omit a detail explanation of the derivation of the transfer functions.

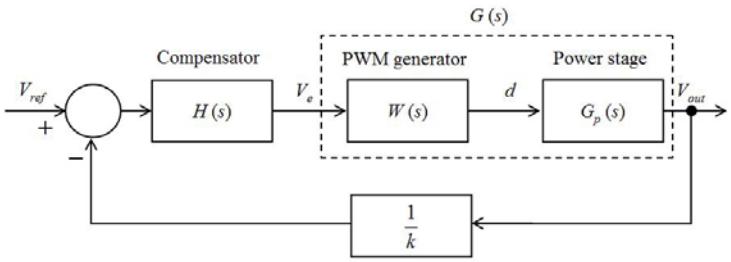


Figure 5.2: Block diagram of the synchronous buck converter.

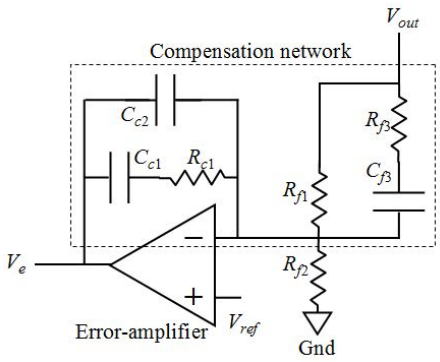


Figure 5.3: Type III-B compensator.

First we derive the transfer function of the power stage (G_p (s)) expressed as Eq. (5-1).

$$G_p(s) = \frac{V_{out}}{d}(s) = \frac{R_{Load}(sC_oR_{ESR}+1)}{s^2L_oC_o(R_{Load}+R_{ESR})+s(L_o+C_oR_{Load}R_{ESR})+R_{Load}} \times V_{in} \quad (5\text{-}1)$$

Under the condition of Eq. (5-2), we obtain Eq. (5-3).

$$R_{Load} >> R_{ESR} \quad (5\text{-}2)$$

$$\frac{R_{Load}}{R_{Load}+R_{ESR}} \approx 1.0 \quad (5\text{-}3)$$

Furthermore, under the condition of Eq. (5-4), we obtain Eq. (5-5).

$$L_o + C_oR_{Load}R_{ESR} << R_{Load} + R_{ESR} \quad (5\text{-}4)$$

$$\frac{(L_o + C_oR_{Load}R_{ESR})}{R_{Load}+R_{ESR}} \approx 0.0 \quad (5\text{-}5)$$

Hence, the denominator in Eq. (5-1) is able to be approximated as given below.

$$
\begin{aligned}
&s^2 L_o C_o \left(R_{Load} + R_{ESR}\right) + s\left(L_o + C_o R_{Load} R_{ESR}\right) + R_{Load} \\
&= \left(R_{Load} + R_{ESR}\right)\left\{ s^2 L_o C_o + s\frac{\left(L_o + C_o R_{Load} R_{ESR}\right)}{R_{Load} + R_{ESR}} + \frac{R_{Load}}{R_{Load} + R_{ESR}} \right\} \\
&\approx \left(R_{Load} + R_{ESR}\right)\left(s^2 L_o C_o + 1\right)
\end{aligned}
\tag{5-6}
$$

Therefore, we rewrite Eq. (5-1) and obtain the following equation (5-7).

$$
G_p(s) = \frac{V_{out}}{d}(s) \cong \frac{R_{Load}\left(sC_o R_{ESR} + 1\right)}{\left(s^2 L_o C_o + 1\right)\left(R_{Load} + R_{ESR}\right)} \times V_{in} \tag{5-7}
$$

The root of the numerator in Eq. (5-7) is the zero of the transfer function of the power stage. Similarly the roots of the denominator in Eq. (5-7) are the poles of the transfer function the power stage. The transfer function of the power stage has a double pole at the resonance frequency of the LC filter, and has a zero produced by the ESR of the output capacitor. The frequency of the double pole and the frequency of the zero are given by Eqs. (5-8) and (5-9), respectively. In particular, the frequency of the zero is an essential parameter of the output capacitor and depends on the kind of the capacitor used.

$$
F_{LC} = \frac{1}{2\pi\sqrt{L_0 C_0}} \tag{5-8}
$$

$$
F_{ESR} = \frac{1}{2\pi C_o R_{ESR}} \tag{5-9}
$$

As mentioned above, the transfer function of the PWM generator ($W(s)$) is expressed as Eq. (5-10). And the power stage including the PWM ($G(s)$) is expressed as Eq. (5-11).

$$
W(s) = \frac{1}{V_{osc}} \tag{5-10}
$$

$$
G(s) = G_p(s) \times W(s) = G_p(s) \times \frac{1}{V_{osc}} \tag{5-11}
$$

The transfer function of the compensator block ($H(s)$) is expressed as Eq. (5-12). Note that it is modeled by the impedance ratio as depicted in Fig. 5.3.

$$
\begin{aligned}
H(s) = \frac{V_e}{V_{out}} &= -\frac{\frac{1}{sC_{C2}} // \left(R_{C1} + \frac{1}{sC_{C1}}\right)}{R_{f1} // \left(R_{f3} + \frac{1}{sC_{f3}}\right)} \\
&= -\frac{\left(sR_{C1}C_{C1} + 1\right) \times \left[sC_{f3}\left(R_{f1} + R_{f3}\right) + 1\right]}{sR_{f1} \times \left(C_{C1} + C_{C2}\right) \times \left[1 + sR_{C1}\left(\frac{C_{C1}C_{C2}}{C_{C1} + C_{C2}}\right)\right] \times \left(sR_{f3}C_{f3} + 1\right)}
\end{aligned}
\tag{5-12}
$$

Under the condition of Eq. (5-13), we obtain the equation (5-14).

$$
C_{C1} >> C_{C2} \tag{5-13}
$$

$$
\frac{C_{C1}C_{C2}}{C_{C1} + C_{C2}} \cong C_{C2} \tag{5-14}
$$

Therefore, we rewrite Eq. (5-12) and obtain the following equation Eq. (5-15).

$$H(s)=\frac{V_e}{V_{out}}\approx-\frac{(sR_{C1}C_{C1}+1)\times\left[sC_{f3}(R_{f1}+R_{f3})+1\right]}{sR_{f1}\times C_{C1}\times(1+sR_{C1}C_{C2})\times(sR_{f3}C_{f3}+1)} \quad (5\text{-}15)$$

The roots of the numerator in Eq. (5-15) are the zeros of the transfer function of the compensator. Similarly the roots of the denominator in Eq. (5-15) are the poles of the transfer function the compensator. Thus, the compensator has two zeros and three poles as given below:

$$F_{Z1}=\frac{1}{2\pi R_{C1}C_{C1}} \quad (5\text{-}16)$$

$$F_{Z2}=\frac{1}{2\pi C_{f3}(R_{f1}+R_{f3})} \quad (5\text{-}17)$$

$$F_{p1}=0 \quad (5\text{-}18)$$

$$F_{p2}=\frac{1}{2\pi R_{f3}C_{f3}} \quad (5\text{-}19)$$

$$F_{p3}=\frac{1}{2\pi R_{C1}C_{C2}} \quad (5\text{-}20)$$

Finally, the transfer function of the whole loop gain of the buck converter depicted in Fig. 5.2 is given below.

$$M(s)=\frac{1}{k}\times H(s)\times\frac{1}{V_{osc}}\times G_p(s)=\frac{1}{k}\times H(s)\times G(s) \quad (5\text{-}21)$$

where $1/k$ represents the gain of the resistor divider that is used in the feedback loop when $V_{out}>V_{ref}$. Note that the effect of this term $1/k$ is considered in Eq. (5-12), and the term is canceled.

5.2.3 MLCC Capacitor

MLCC (Multi Layer Ceramic Capacitor) capacitors are a kind of output capacitors [5] [33]-[35]. They are used in the buck DC-DC converters using the type III-B compensator [1] [3] [4].

The MLCC capacitor is modeled as a serial connection that is composed of an effective capacitance and a stray resistance called ESR (equivalent series resistance). This model is an equivalent circuit depicted in Fig. 5.4. The gain of the loop compensation is largely dependent upon the effective capacitance. And the phase margin is largely dependent upon the ESR. Therefore, in the circuit design of DC/DC converters, an optimal output capacitor is needed in order to stabilize the loop [5] [33]-[35].

In the following discussion, for simplification, we assume that the characteristics of MLCC capacitor do not depend on its operating condition such as frequency, temperature, and voltage.

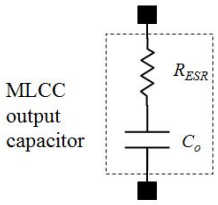


Figure 5.4: Equivalent circuit model of the MLCC capacitor.

5.3 Implementation

We implement the above derived transfer functions (Eqs. (5-7), (5-10), (5-11), (5-15), (5-21)), the frequencies of zeros (Eqs. (5-9), (5-16), (5-17)), and the frequencies of poles (Eqs. (5-8), (5-18), (5-19), (5-20)) into Scilab. Scilab is free and open source software for numerical computation providing a powerful computing environment for engineering and scientific applications [30]. In the implementation, we use the transfer function representations of Scilab.

The main purpose of this work is to find an optimal MLCC capacitor that satisfies the circuit design specification of DC/DC converter. First we check the characteristic listed in the data sheet of the MLCC used in the circuit design. Next we sweep the value of effective capacitance of MLCC capacitor, and obtain the corresponding value of ESR. At each combination of ESR and effective capacitance, we calculated the transfer functions mentioned above and obtain the corresponding frequency response in the form of Bode Plot. We repeat this calculation process, and obtain an optimal MLCC capacitor finally. Thus our optimization technique is very simple.

5.4 Experimental Results

As described above, we derived the system of transfer functions. We develop a source code and implement it into Scilab. The values of main parameters are set in the following: V_{in}=12 [V], V_{out}=1.8 [V], V_{ref}=0.7 [V], V_{osc}=1.8 [V], L_o=1.5e-6 [H], C_o=4 × 10.8e-6=43.2e-6 [F], R_{ESR}=3e-3/4=0.75e-3 [Ohm], F_s=600e3 [Hz], I_o=4.0 [A], R_{Load}=1.0 [Ohm].

Furthermore, the value of each design parameter in the system of transfer functions is set based on the datasheet and application note [1], which are indicated by International Rectifier [28]. We determine the design parameters in the following procedure.

The poles and zeros of the power stage are calculated by using Eqs. (5-8) and (5-9):

$$F_{LC} = \frac{1}{2\pi\sqrt{43.2\text{e}-6\times 1.5\text{e}-6}} = 19.7\text{e}3\,[\text{Hz}] \tag{5-22}$$

$$F_{ESR} = \frac{1}{2\pi\times 43.2\text{e}-6\times 0.75\text{e}-3} = 4.9\text{e}6\,[\text{Hz}] \tag{5-23}$$

The zero cross frequency is set to 1/6 of the switching frequency:

$$F_0 = \frac{F_s}{6} = \frac{600\text{e}3}{6} = 100\text{e}3\,[\text{Hz}] \tag{5-24}$$

Therefore, the frequency condition of type III-B compensator [1] is satisfied as depicted in Eq. (5-25).

$$F_{LC} < F_0 < F_s/2 < F_{ESR} \tag{5-25}$$

The poles and zeros of the compensator are calculated as given below [1]. Note that the maximum phase lead (Θ) of the compensator is set to 70 degree.

$$F_{p3} = \frac{F_s}{2} = 300\text{e}3[\text{Hz}] \tag{5-26}$$

$$F_{Z2} = F_0 \times \sqrt{\frac{1-Sin\theta}{1+Sin\theta}} = F_0 \times \sqrt{\frac{1-Sin(70)}{1+Sin(70)}} = 17.6\text{e}3[\text{Hz}] \tag{5-27}$$

$$F_{P2} = F_0 \times \sqrt{\frac{1+Sin\theta}{1-Sin\theta}} = F_0 \times \sqrt{\frac{1+Sin(70)}{1-Sin(70)}} = 567\text{e}3[Hz] \tag{5-28}$$

$$F_{Z1} = \frac{F_{Z2}}{2} = 8.8\text{e}3[\text{Hz}] \tag{5-29}$$

Under the frequency condition mentioned above, we calculate the values of the design parameters of the compensator. First we set the value of parameter C_{f3} to 2.2e-9 farad. The value of parameter R_{f3} is calculated as given below by using Eq. (5-19).

$$R_{f3} = \frac{1}{2\pi C_{f3} F_{P2}} = \frac{1}{2\pi \times 2.2\text{e}-9 \times 567\text{e}3} = 127.6[\text{Ohm}] \tag{5-30}$$

We choose $R_{f3} = 127[\text{Ohm}]$. The value of parameter R_{f3} is calculated as given below by using Eq. (5-17).

$$R_{f1} = \frac{1}{2\pi C_{f3} F_{z2}} - R_{f3} = \frac{1}{2\pi \times 2.2\text{e}-9 \times 17.6\text{e}3} - 127 = 3.98e3[\text{Ohm}] \tag{5-31}$$

We select $R_{f1} = 4.02\text{e}3[\text{Ohm}]$. The value of parameter R_{f2} is calculated as given below by using Eq. (5-32) [1].

$$R_{f2} = \frac{R_{f1} \times V_{ref}}{V_{out} - V_{ref}} = \frac{4.02\text{e}3 \times 0.7}{(1.8-0.7)} = 2.56e3[\text{Ohm}] \tag{5-32}$$

We choose $R_{f2} = 2.55\text{e}3[\text{Ohm}]$. The value of parameter R_{c1} is calculated as given below by using Eq. (5-33) [1].

$$R_{c1} = \frac{2\pi \times F_0 \times L_o \times C_o \times V_{osc}}{V_{in} \times C_{f3}} = \frac{2\pi \times 100\text{e}3 \times 1.5\text{e}-6 \times 43.2\text{e}-6 \times 1.8}{12.0 \times 2.2\text{e}-9} = 2.77e3[\text{Ohm}] \tag{5-33}$$

We choose $R_{c1} = 2.74e3[\text{Ohm}]$. The value of parameter C_{c1} is calculated as given below by using Eq. (5-16).

$$C_{c1} = \frac{1}{2\pi \times R_{c1} \times F_{z1}} = \frac{1}{2\pi \times 2.74\text{e}3 \times 8.8\text{e}3} = 6.6\text{e}-9[\text{F}] \quad (5\text{-}34)$$

We choose $C_{c1} = 6.8\text{e}-9[\text{F}]$. The value of parameter C_{c2} is calculated as given below by using Eq. (5-20).

$$C_{c2} = \frac{1}{2\pi \times R_{c1} \times F_{p3}} = \frac{1}{2\pi \times 2.74\text{e}3 \times 300\text{e}3} = 193e-12[\text{F}] \quad (5\text{-}35)$$

Finally we choose $C_{c2} = 180e-12[\text{F}]$.

Fig. 5.5 show an example of our implementation using the transfer function representations of Scilab. Fig. 5.5 (a) depicts the source code.

As our experimental verification, we ran the simulation source code with Scilab on HP dv9700 (OS Windows 7, CPU Intel(R) Core(TM) 2.5GHz, RAM 8.00 GB). It run time (CPU time) is 2.1 second. Figure 5.5 (b) depicts the simulation results in the frequency domain. The zero crossover frequency is about 1.05e5 Hz. The gain margin is 18.759 degree. The phase margin is 50.474 degree.

As other reference, we ran frequency-domain simulation in netlist-level on a power electronics circuit simulator, which is called as SIMPLIS [27]. The simulated circuit of a buck DC/DC converter is depicted in Fig. 5.6 (a). Note that this circuit is equivalent to the system of transfer functions described above. In this case, the run time with the same computer mentioned above is 150.9 second. Fig. 5.6 (b) depicts the circuit simulation results obtained by SIMPLIS. The zero crossover frequency is about 1.13e5 Hz. The gain margin is 13.461 degree. The phase margin is 49.595 degree. Thus the simulation results of our equation-based modeling are almost consistent with those of SIMPLIS. Hence it demonstrates the adequacy of our equation-based circuit design technique. And our technique is 70 times faster than SIMPLIS.

Table 5.1 demonstrates the simulation results in the various cases of the combination of ESR and effective capacitance of the MLCC capacitor based on the datasheet [5], which are indicated by TDK-EPC Corporation. Particularly, in the case of (1), the power electronics circuit simulator SIMPLIS is not able to simulate it (no-convergence). On the other hand, our technique can deal with the same case.

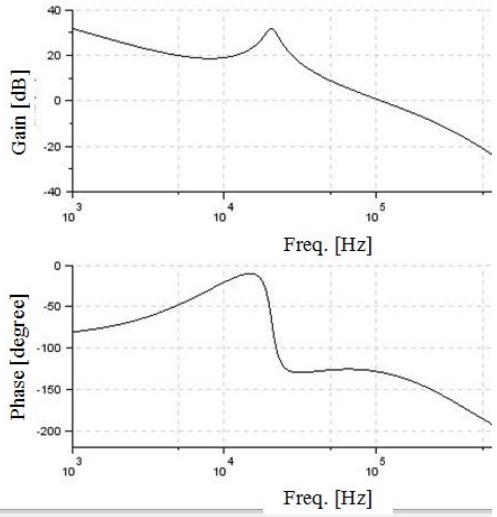
The results reveal the superiority of our technique. They also demonstrate that our technique is able to be applied to industrial design of DC/DC converter.

5.5 Conclusions

We have proposed a new technique of equation-based circuit design for DC/DC converters. It starts with the modeling of the frequency response of a buck DC/DC converter with a loop compensation, and derive the governing equation of ESR. It then determines the optimal MLCC capacitor that satisfies the design specification of the converter. Furthermore, we applied the technique into the circuit design of a practical industrial buck DC/DC converter. Our technique was demonstrated by experimental results. They also revealed that the technique has the capacity of dealing with the practical industrial design/analysis, and its performance is comparable to that of a power electronics circuit simulator.

In the future work, we have a plan to extend the technique in order to be able to deal with the characteristics on time domain such as output voltage ripple, transient response.

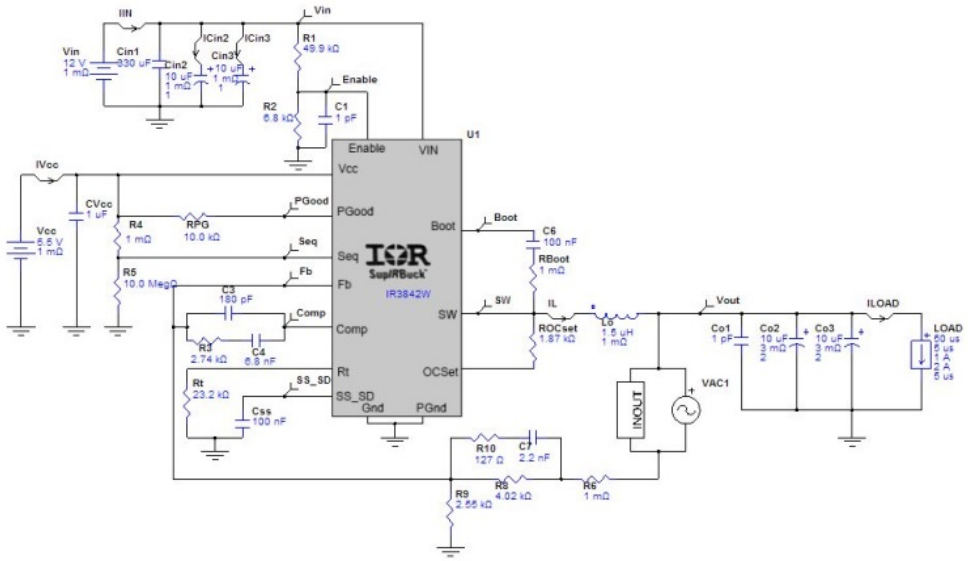
```
//-
//-Circuit-Parameters
//-
L0=1.5e-6 //[H]
C0=43.2e-6 //[F]
ESR=0.75e-3 //[Ohm]
RLOAD=1.0 //[]
VIN=12.0 //[V]
VOSC=1.8 //[V]
//-
Cf3=2.2e-9 //[F]
Rf3=127.0 //[Ohm]
Rf1=4.02e3 //[Ohm]
Rf2=2.55e3 //[Ohm]
RC1=2.74e3 //[Ohm]
CC1=6.8e-9 //[F]
CC2=180e-12 //[F]
//
//-Transfer-Funtion
//
s=poly(0,'s');
//Gp:-transfer-function-of-a-power-stage-and-PWM-control
Gp=(RLOAD*(C0*ESR*s+1)*VIN)/(L0*C0*s*s*(RLOAD+ESR)+s*(L0+RLOAD*C0*ESR)+RLOAD) //Gp
//H:-transfer-function-of-a-type-III-A-compensator
H=(1.0+s*RC1*CC1)*(1.0+s*Cf3*(Rf1+Rf3))/(s*Rf1*CC1*(RC1*CC2*s+1.0)*(1.0+s*Rf3*Cf3))
//G:-transfer-function-of-a-switiching-feedback-loop
G=H*(Gp/VOSC)
sys=syslin('c',G);
//
//-Transient-Analysis
//
t=linspace(0,1.0e-3,10000);
y=csim('step',t,sys);
//
//-ac-analysis
//
xgrid()
xtitle('Freq.-Respons','freq(Hz)','Gain/Phase')
bode(sys,1e3,1e6,0.001)
g_margin(sys)
p_margin(sys)
//
```



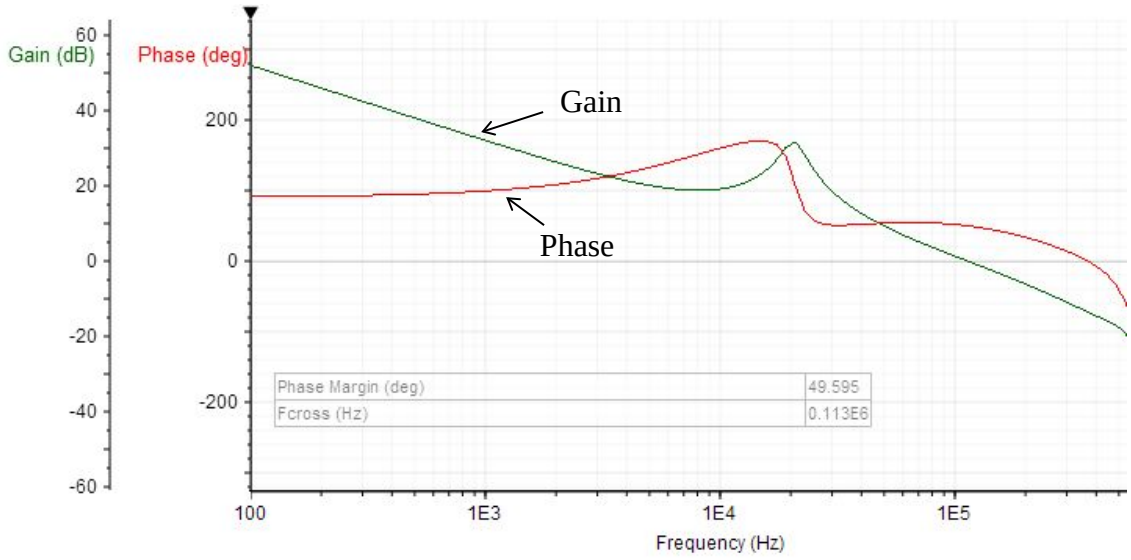

```
-->g_margin(sys)
 ans  =

    18.759007
-->p_margin(sys)
 ans  =

    50.474232
```

(a) Simulation source code (b) Simulation result

Figure 5.5: Our implementation using the transfer function representation of Scilab.



(a) Schematic



(b) Simulation result

Figure 5.6: Simulation using SIMPLIS

Table 5.1: Simulation results in the various cases of the combination of ESR and effective capacitance.

Case	C_o [μF]	R_{ESR} [mOhm]	Scilab			SIMPLIS		
			Crossover frequency [Hz]	Gain margin [degree]	Phase margin [degree]	Crossover frequency [Hz]	Gain margin [degree]	Phase margin [degree]
(1)	3.0	6.0	2.50E+05	8.044	25.020	NG	NG	NG
(2)	8.0	4.5	1.50E+05	17.219	47.857	1.390E+05	10.825	45.666
(3)	10.0	3.0	1.05E+05	18.759	50.474	1.130E+05	13.461	49.595
(4)	30.0	1.5	4.00E+04	29.076	47.473	4.200E+04	25.558	48.977

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Chapter 6
Efficient Large-Scale Power Grid Analysis with Parallel Computing

6.1 Introduction

Due to the increasing complexity and power consumption of LSI chips, power grid analysis is an important issue. A robust power network design has to guarantee the correctness of circuit functionalities without slowing down operations. An improper design of power grid (power distribution system) can result in excessive IR-drop (resistive voltage drop), and fluctuations in the voltages supplied to the active devices (transistors, functional blocks, etc.). If the voltage drop becomes too large, it increases the gate delays and causes logical errors (functional failures). And it degrades the circuit reliability. Many researchers have studied the impact, and proposed solutions to the problem [1] [13].

So far circuit simulators such as SPICE [11] and GridSim [6] have been used for power grid analysis in the LSI design. And some high performance numerical solvers also were developed [3] [4] [7] [14] [15].

Mathematica is worldwide software of symbolic analysis (computer algebra) and a numerical analysis tool, and it is used in science, engineering, mathematics, and other areas [8]. In the area of electronic/electrical design, Mathematica has been applied to symbolic circuit analysis for analog circuits [5] [9], and numerical analysis for a power MOSFET circuit [10]. Furthermore, in the Wolfram Demonstrations Project, some examples of equation-based modeling for very simple electronic circuits were exhibited [2]. Recently Mathemtica also supports a parallel computing method [12].

The goal of our study is to propose a technique for large scale power grid analysis with Mathematica. There are two supply grids in LSI design: the power and ground grids. The two grids influence each other, and therefore a simultaneous simulation is preferred. However, if we take advantage of the fact that the power and ground grids are often symmetric, the combined power/ground grids can be reduced back to a single power grid [1] [13] [15]. Therefore, in this paper, we consider the analysis of the power grid. Furthermore we deal with the IR-drop which is mostly due to the voltage drop due to power line resistances on chip. First we consider a RC circuit model that is composed of a large scale linear interconnect network and the driving current sources due to the active devices in the power grid, and express it as a system of ordinary differential equations. Next we implement the system into Mathematica, and solve it. In particular, we perform verification for the IR-drop values under the condition of various driving currents with parallel computing method. Finally we demonstrate our technique by several test results.

In the next section, we explain a RC elements network model of the power grid and derive the system of ordinary differential equations. Section 6.3 describes our technique for the power grid analysis and implements it into Mathematica. Section 6.4 describes our experiments and compares the results. We conclude our research in Section 6.5.

NOMENCLATURE

t	Simulation time domain [sec]
(i,j)	Coordinate system of power grid (The index i and j ranges as $i = 1, 2, \ldots, m$; $j = 1, 2, \ldots, n$)
m	A positive integer of 2 or more

n	A positive integer of 2 or more
$v_{i,j}$	Nodal voltage at node (i,j) [V]
C_{int}	Interconnect capacitance [F]
R_{int}	Interconnect resistance [Ohm]
G_{int}	Interconnect conductance [1/Ohm] (G_{int}=1/ R_{int})
R_{off}	Off resistance of active device [Ohm]
G_{off}	Off conductance of active device [1/Ohm] (G_{off}=1/ R_{off})
$I_{i,j}$	Pulsed driving current of active device at node (i,j) [A]
I_{high}	High value of pulsed driving current [A] (I_{high}=*Max* ($I_{i,j}$))
I_{low}	Low value of pulsed driving current [A] (I_{low}=*Min* ($I_{i,j}$))
Max ()	Maximum function
Min ()	Minimum function
C_M	Capacitance matrix : C_M=[C_{int}]
G_M	Conductance matrix : G_M =[G_{int}]+[G_{off}]
I_M	Pulsed driving current matrix : I_M=[$I_{i,j}$]
v_M	Nodal voltage vector : v_M =[$v_{i,j}$]
V_{dd}	Power supply voltage [V]
T_{sw}	Switching pulse period [sec]

6.2 The Problem

Consider a simple power grid as depicted in Fig. 6.1. The power grid is a mesh structure, in which each edge is modelled as a uniform interconnect resistance. Each node ($v_{i,j}$) in the mesh has a uniform parasitic capacitance (C_{int}) to the ground. Active devices are modelled as pulsed current sources, and are connected to the mesh nodes. Each pulsed current source ($I_{i,j}$) is a driving current to be generated by the switching of the active device. Note that each driving current source has an off resistance (R_{off}) in parallel. Four corner nodes are connected to power pads (power supply voltage sources) that can be treated as ideal voltage sources (V_{dd}). Therefore our simple power grid is composed of a linear network of uniform distributed RC elements which excited by 4-corner ideal voltage sources and driving current sources.

Therefore our simple power grid is composed of a linear network of uniform distributed RC elements which excited by 4-corner ideal voltage sources and driving current sources. As depicted in Fig. 6.2, the KCL (Kirchhoff's Current Law) with respect to each node is expressed as Eq. (6-1).

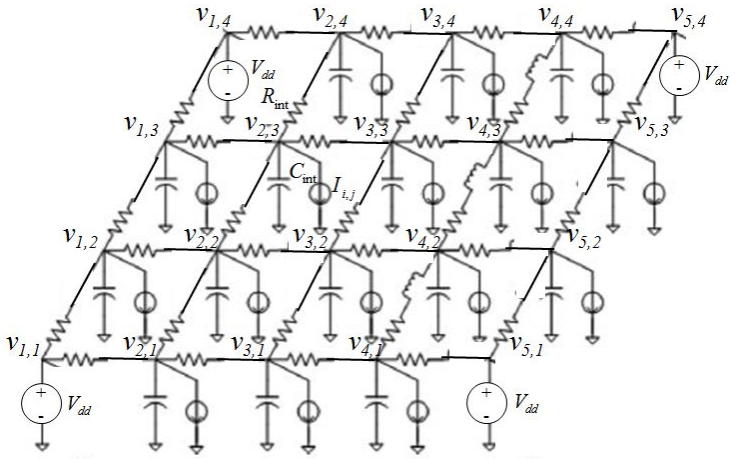


Figure. 6.1: Power grid schematic. This example is a case of grid size 5x4 (m=5, n=4).

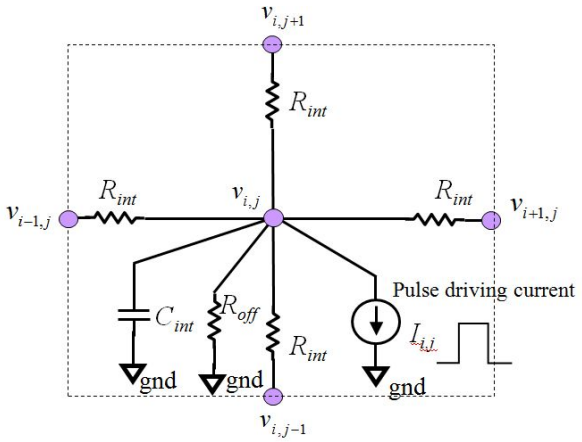


Fig. 6.2: KCL with respect to each node in the power grid.

$$C_{\text{int}}\frac{dv_{i,j}}{dt}=\frac{v_{i-1,j}-v_{i,j}}{R_{\text{int}}}+\frac{v_{i+1,j}-v_{i,j}}{R_{\text{int}}}+\frac{v_{i,j-1}-v_{i,j}}{R_{\text{int}}}+\frac{v_{i,j+1}-v_{i,j}}{R_{\text{int}}}-\frac{v_{i,j}}{R_{off}}-I_{ij} \tag{6-1}$$

We rewrite Eq. (6-1) and get the following equation.

$$C_{\text{int}}\frac{dv_{i,j}}{dt}=G_{\text{int}}\left(v_{i-1,j}-v_{i,j}\right)+G_{\text{int}}\left(v_{i+1,j}-v_{i,j}\right)+G_{\text{int}}\left(v_{i,j-1}-v_{i,j}\right)+G_{\text{int}}\left(v_{i,j+1}-v_{i,j}\right)-G_{off}v_{i,j}-I_{ij} \tag{6-2}$$

Hence the whole of the linear network can be represented as a system of ordinary differential equations, which is expressed as Eq. (6-3). Our problem is to find the IR-drop and fluctuations in the voltages supplied to the active devices on chip by solving the system of Eq. (6-3). Note the matrix form of Eq. (6-3).

$$C_M\frac{dv_M}{dt}=G_Mv_M-I_M \tag{6-3}$$

6.3 Implementation into Mathematica

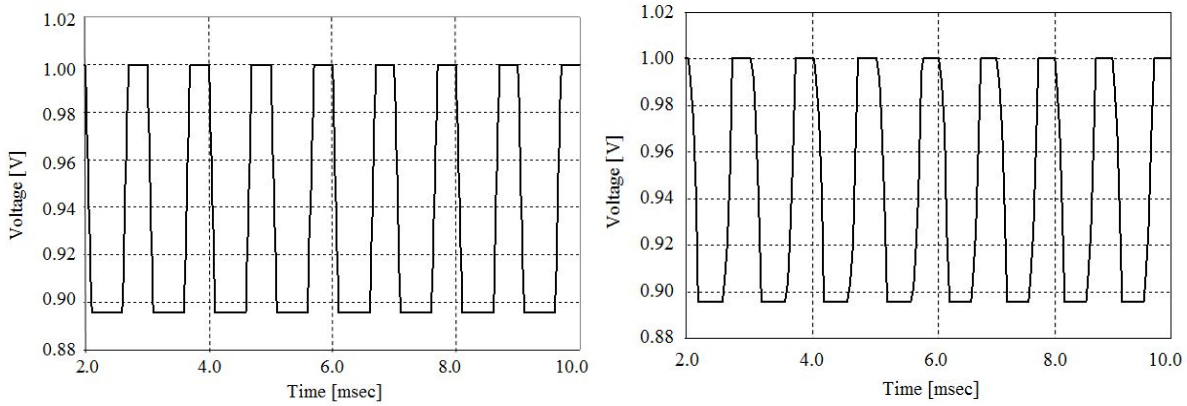
As described above, in our technique, we formulated the problem of the power grid analysis and derived the system of ordinary differential equations which expressed as Eq. (6-3). We develop a notebook source code to solve the system by using a numerical solver called NDsolve(), and implement it into Mathematica. In order to verify the results from the analysis with our technique, we compare with those from SPICE simulation.

In the remainder of this paper, we consider the stochastic behaviour of the switching of the active devices on chip and place the driving current sources at random with using random numbers. And we assume the synchronous switching of the active devices in the power grid.

As our experimental verification, we set the values of the main parameters as following:

I_{high}=2.0e-5 [A], I_{low}=0.0 [A], R_{int}=25.0 [Ohm], C_{int}=3e-16 [F], R_{off}=1.0e12 [Ohm], T_{sw}=1.0e-3 [sec], V_{dd}=1.0 [V], m=30, n=30. First we ran the power grid analysis with Mathematica-8 on HP dv9700 (OS Windows 7, CPU Intel(R) Single Core(TM) 2.5GHz, RAM 8.00 GB). And we obtained the nodal voltages of the power grid, and its run-time (CPU time) is 91.2 [sec]. Fig. 6.3 (1) depicts the voltage fluctuations at the node $v_{15,15}$ in the time domain.

As other reference, we use a general-purpose circuit simulator known as Ngspice [11] (gEDA Project version of SPICE), and simulate the RC-elements network of the same power grid. In this case, the run-time with the same computer mentioned above is 4.54 [sec]. Fig. 6.3 (2) depicts the voltage fluctuations at the node $v_{15,15}$ which obtained by Ngspice.



(1) Our technique with Mathematica (2) Ngspice

Figure 6.3: Voltage fluctuations at the node $v_{15,15}$.

The results from the analysis with our technique are in accord with those from SPICE simulation. Thus the results demonstrate that our technique is capable of the same analysis as SPICE, and is applicable to power grid design of LSI chips.

6.4 Experimental Results

In the power grid design, the verification for the IR-drop values under the condition of various driving currents is very essential. We apply the technique described as above to the verification, and use the parallel computing method in Mathematica, in the sake of its efficiency. Fig.6.5 depicts an example of our notebook source code which used the parallel computing method.

In the first experimentation, on the power grid of the 20x20 grid nodes (m=20, n=20), we consider the case in which the value of the pulsed driving current (I_{high}) takes the range from 1.0e-5 to 8.0e-5 which its step size is 1.0e-5. Note that the values of other parameters are same as those in Section III. We ran the power grid analysis for each case at the same time, with Mathemtica-8 on SUSE Linux Enterprise Server 11 which is composed of Intel Xeon Processor (8-core, 2.0GHz) and SGI Performance Suite software. Its run-time is 29.36 [sec], and is 3.79 times faster than that (111.27[sec]) of the sequential computing method in Mathemtica. Table 6.1 shows the IR-drop value at the node $v_{10,10}$ for each pulsed driving current. Furthermore, the IR-drop values from Mathemtica are in accord with that of those from Ngspice. The relative error is less than 2 percent. This supports the correct IR-drop values which produced by our technique. And it also indicates the effectiveness of the parallel computing method in the power grid optimization design.

Table 6.1: IR-drop values at the node $v_{10,10}$ under the condition of various driving currents pulsed driving current.

Driving Current I_{high} [A]	(1) Mathemtica IRdrop [V]	(2) Ngspice IRdrop [V]	Reative Error ((1)-(2))/(2) [%]
1.00E-05	0.0194	0.0194	0.000
2.00E-05	0.0385	0.0387	-0.517
3.00E-05	0.0578	0.0588	-1.701
4.00E-05	0.0779	0.0774	0.646
5.00E-05	0.0963	0.0968	-0.517
6.00E-05	0.1169	0.1162	0.602
7.00E-05	0.1364	0.1355	0.664
8.00E-05	0.1541	0.1549	-0.516

In the second experimentation, under the same condition as that of the first experimentation described as above, we evaluate the performance of our technique. Table 6.2 and Fig.6.4 show the CPU time for each size (m x n) of the power grid. The processing CPU time of Mathematica is proportional to the 2.5 power of grid size m (=n). On the other hand, that of Ngspice is proportional to the 3 power of the grid size m. Note that the difference of CPU time between Mathemtica and Ngspice becomes less in the case of large scale grid. Especially, Mathemaica is able to analyze the power grid under the condition of grid size m=n=300. But Ngspice is unable to deal with it due to memory.

The results reveal the superiority of our technique under the condition of very large scale power grids. They also demonstrate that our technique is able to be applied to industrial design of power grid of LSI chips in a practical time.

Table 6.2: CPU time for different size of power grid.

m	n	(1) Mathemtica (Parallel Computing)		(2) Ngspice		(1) / (2) CPU Time Ratio [-]
		CPU Time [sec]	Ratio [-]	CPU Time	Ratio [-]	
10	10	4.92	1.00	0.29	1.00	17.1
20	20	29.36	5.97	1.68	5.83	17.5
30	30	72.90	14.82	6.98	24.22	10.4
40	40	144.68	29.41	19.14	66.44	7.6
50	50	259.48	52.75	55.34	192.14	4.7
75	75	650.80	132.30	274.46	953.00	2.4
100	100	1480.68	301.01	912.60	3168.75	1.6
200	200	8799.37	1788.85	7142.40	24800.00	1.2
300	300	24260.27	4930.95	NG	NG	—

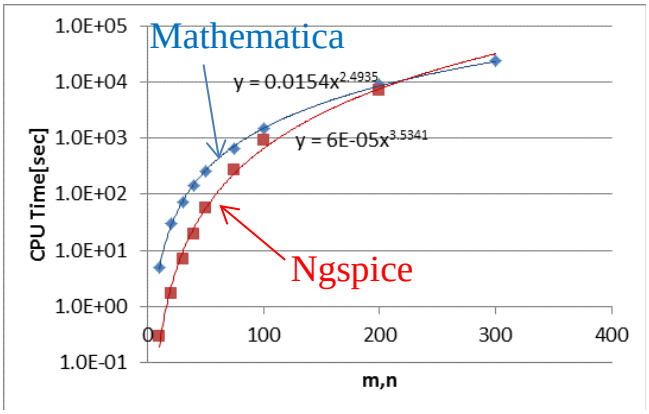


Figure 6.4: CPU time for different size of power grid.

6.5 Conclusions

We proposed a technique for large scale power grid analysis with a parallel computing method in computer algebra system. We modeled a power grid as a system of ordinary differential equations, and applied the parallel computing method in Mathemtica to obtain the solution efficiently. We explained the technique using a linear RC elements network model as the power grid. Our experimental results demonstrated that the technique is capable of the time domain analysis just the same as SPICE, a general-purpose circuit simulator, and is applicable to power grid design of LSI chips. We also revealed the superiority of our technique for the power grids of very large scale, and also indicated the effectiveness of the parallel computing method in the power grid optimization design. In the future work, we plan to extend the technique to be able to deal with RLC interconnect network with parasitic inductive effects, and develop a new parallel numerical solver to achieve more high performance.

```
(*** Pulse function ***)
fpulse[x_Real,delay_,rise_,width_,fall_,periode_,lowval_,highval_]=Which[x<=delay,lowval,Mod[x-delay,periode]>rise+width+fa
ll,lowval,Mod[x-delay,periode]>rise+width,(lowval-highval)/fall*(Mod[x-delay,periode]-rise-width)+highval,Mod[x-delay,periode
]>rise,highval,Mod[x-delay,periode]>0.0,(highval-lowval)/rise*(Mod[x-delay,periode])+lowval,Mod[x-delay,periode]<=0.0,lowva
l];

(*** Size: 20 x 20 ***)
Clear [v2xy1, v3xy1, v4xy1, v5xy1, v6xy1,
 .
 .
 .
v15xy20, v16xy20, v17xy20, v18xy20, v19xy20] ;

(*** A system of ordinary differential equations ***)
eqns={cint v2xy1'[t]==-v2xy1[t]/roff+(v1xy1-v2xy1[t])/rint+(v3xy1[t]-v2xy1[t])/rint+(v2xy2[t]-v2xy1[t])/rint,
cint v3xy1'[t]==(-1) isrc
fpulse[t,0+delay,rise,width,fall,periode,lowval,highval]-v3xy1[t]/roff+(v2xy1[t]-v3xy1[t])/rint+(v4xy1[t]-v3xy1[t])/rint+(v3xy2[t]-
v3xy1[t])/rint,
   cint v4xy1'[t]==(-1) isrc
fpulse[t,0+delay,rise,width,fall,periode,lowval,highval]-v4xy1[t]/roff+(v3xy1[t]-v4xy1[t])/rint+(v5xy1[t]-v4xy1[t])/rint+(v4xy2[
t]-v4xy1[t])/rint,
cint v5xy1'[t]==(-1) isrc
fpulse[t,0+delay,rise,width,fall,periode,lowval,highval]-v5xy1[t]/roff+(v4xy1[t]-v5xy1[t])/rint+(v6xy1[t]-v5xy1[t])/rint+(v5xy2[t]-
v5xy1[t])/rint,
cint v6xy1'[t]==(-1) isrc
```

```
fpulse[t,0+delay,rise,width,fall,periode,lowval,highval]-v6xy1[t]/roff+(v5xy1[t]-v6xy1[t])/rint+(v7xy1[t]-v6xy1[t])/rint+(v6xy2[t]-
v6xy1[t])/rint,
 .
 .
 .
cint v15xy20'[t]==-v15xy20[t]/roff+(v14xy20[t]-v15xy20[t])/rint+(v16xy20[t]-v15xy20[t])/rint+(v15xy19[t]-v15xy20[t])/rint,
cint v16xy20'[t]==-v16xy20[t]/roff+(v15xy20[t]-v16xy20[t])/rint+(v17xy20[t]-v16xy20[t])/rint+(v16xy19[t]-v16xy20[t])/rint,
cint v17xy20'[t]==-v17xy20[t]/roff+(v16xy20[t]-v17xy20[t])/rint+(v18xy20[t]-v17xy20[t])/rint+(v17xy19[t]-v17xy20[t])/rint,
cint v18xy20'[t]==-v18xy20[t]/roff+(v17xy20[t]-v18xy20[t])/rint+(v19xy20[t]-v18xy20[t])/rint+(v18xy19[t]-v18xy20[t])/rint,
cint v19xy20'[t]==-v19xy20[t]/roff+(v18xy20[t]-v19xy20[t])/rint+(v20xy20-v19xy20[t])/rint+(v19xy19[t]-v19xy20[t])/rint,

v2xy1[0]==0, v3xy1[0]==0, v4xy1[0]==0, v5xy1[0]==0, v6xy1[0]==0,
 .
 .
 .
v15xy20[0]==0, v16xy20[0]==0, v17xy20[0]==0, v18xy20[0]==0, v19xy20[0]==0};

eqns=eqns/.{cint->3/10000000000000000,roff->1000000000000,rint->25,v1xy1->1,v1xy20->1,v20xy1->1,v20xy20->1,delay->0,r
ise->1/10000,width->5/10000,fall->1/10000,periode->10/10000,lowval->0,highval->1};

(*** Parallel computing ***)
sol:=ParallelTable[NDSolve[eqns,{v2xy1, v3xy1, v4xy1, v5xy1, v6xy1
 .
 .
 .
v15xy20, v16xy20, v17xy20, v18xy20, v19xy20},
{t,0,10 10/10000},MaxStepSize->1/10000,MaxSteps->1000000],{isrc,1/10000,8/10000,1/10000}];

DistributeDefinitions[sol];

(*** Evaluation and Plot graph ***)
Table[Plot[Evaluate[v10xy10[t]/.sol[[i]]],{t,0,10 10/10000},PlotLabel->isrc],{i,1,Length[sol],1}]
```

Figure 6.5: Our notebook source codes with parallel computing method in Mathematica

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Chapter7
Conclusions

We presented symbolic and numerical computational approach to design of LSI circuits as their industrial application.

Our proposed design approach is an equation-based method such that the circuit behavior and characteristics are represented as a mathematical model. By equation-based analysis of the circuit behavior and characteristics, it is possible to understand quantitatively the effect of parameters on the properties. Our proposed method is to model circuit behavior and characteristics by equations and solve them with constraints and specifications using generic symbolic computational system. The generic symbolic computational system has both symbolic and numerical calculation functions. Therefore we researched the case of both symbolic and numerical calculation to obtain the solutions of the equations.

At first, we focused on importance of signal delay in digital design, and we applied the symbolic computation to estimate the signal delay. We modeled delay characteristic by a polynomial and designed 1-bit full adder circuit by using proposed method. In addition, we expanded to the analysis of the signal delay in consideration of the temperature rise due to Joule heating in interconnects. As a result, we confirmed the effectiveness of our proposed method for the transient analysis that is the basis of the digital circuits design.

Next, we presented two applications to frequency analysis that is very important in analog circuits design. The first application is to optimize the parameters of the power loop circuit that is a core of power supply system. We derived the transfer function of the power supply loop circuit and determined the most suitable circuit parameters to satisfy design target. To obtain these parameters, we tried to solve a system of nonlinear equations by using symbolic and numerical computation. As a result, we obtained valid solutions with symbolic computation. The second application is to obtain design parameters of the DC/DC converter which is a representative power supply circuit. We derived the transfer function representing the behavior of whole system. Especially, we focused on that capacitance of the output capacitor and parasitic resistance among the design parameters have effects on the frequency characteristics and circuit stabilization of the DC/DC converter, so we applied our equation-based design and optimized design parameters with numerical computation. Our experimental results demonstrated that our technique makes possible to solve the case which cannot be solved by conventional power electronics circuit simulator. Also, calculation speed by our proposed method was 80 times faster than the conventional method, so our proposed method demonstrated the utility and efficiency.

Furthermore, we suggested a modeling of an equation-based electro-thermal coupling of power MOSFETs for predicting reliability by using numerical calculation. In view of this experimental result, we presented that our proposed method is applicable to not only digital circuits transient analysis or analog circuits frequency analysis, but also power MOSFETS reliability evaluation.

Finally, we proposed a technique for large scale power grid analysis with a parallel computing method in computer algebra system. We modeled a power grid as a system of ordinary differential equations, and applied the parallel computing method to obtain the solution efficiently. We explained the technique using a linear RC elements network model as the power grid. Our experimental results demonstrated that the technique is capable of the time domain analysis just the same as SPICE, a general-purpose circuit simulator, and is applicable to power grid design of LSI chips. We also revealed the superiority of our technique for the power grids of very large scale, and also indicated the effectiveness of the parallel computing method in the power grid optimization design.

In our research, we achieved to improve the efficiency and the accuracy of design by

modeling the circuit behavior and characteristics through equations and solving with symbolic or numerical computation in the early stages of LSI design. In other words, we contributed to improve the efficiency and the accuracy in the semiconductor and LSI design field. As a next step, we want to apply to the design of more large-scale circuits. In our future work, we intend to apply an equation-based approach to analyze and design of various systems of science and engineering and industrial field.

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